## TABLE OF CONTENTS

1. OUTLINE OF LCD MODULE .............................................................................................................................................. 4
   1.1 FEATURES .................................................................................................................................................................. 4

2. SPECIFICATION ........................................................................................................................................................................ 5
   2.1 MAXIMUM RATINGS ....................................................................................................................................................... 5
   2.2 ELECTRICAL CHARACTERISTICS .................................................................................................................................. 6
   2.3 LCD DRIVING VOLTAGE AND CONNECTION .................................................................................................................. 7
   2.4 EL BACK LIGHT ............................................................................................................................................................... 9
   2.5 CCT BACK LIGHT ............................................................................................................................................................ 10

3. INTERFACE .............................................................................................................................................................................. 11
   3.1 INTERFACE CONNECTION ................................................................................................................................................ 11
   3.2 BLOCK DIAGRAM ............................................................................................................................................................ 16
   3.3 SIGNAL TIMINGS ............................................................................................................................................................... 17
   3.4 MEMORY ADDRESS AND DISPLAY POSITION .................................................................................................................. 18
      3.4.1 Memory Address and Display Position .................................................................................................................... 18
      3.4.2 Memory Address and Display Position .................................................................................................................... 20
      3.4.3 RAM Map ............................................................................................................................................................... 22

4. SOLDERING JUMPER SETTING ............................................................................................................................................ 23
   4.1 INITIAL SETTING ............................................................................................................................................................ 23
   4.2 EXPLANATION OF EACH SOLDERING JUMPER ................................................................................................................ 24

5. COMMUNICATION BETWEEN CPU AND MODULE ................................................................................................................... 26
   5.1 DATA TRANSMISSION METHOD ....................................................................................................................................... 26
      5.1.1 Status Read ............................................................................................................................................................ 27
   5.2 COMMAND ........................................................................................................................................................................ 28
      5.2.1 Command List ......................................................................................................................................................... 28
      5.2.2 Description of Command .......................................................................................................................................... 32
      5.2.2.1 Pointer Set Command ........................................................................................................................................... 32
      5.2.2.2 Control Word Set Command .................................................................................................................................. 33
      5.2.2.3 Mode Set Command ............................................................................................................................................. 34
      5.2.2.4 Display Mode Set Command .................................................................................................................................. 35
      5.2.2.5 Cursor Pattern Select Command .............................................................................................................................. 36
      5.2.2.6 Data Auto Write/Data Auto Read ............................................................................................................................. 36
      5.2.2.7 Data Write/Data Read ........................................................................................................................................ 38
      5.2.2.8 Screen Parking .................................................................................................................................................... 38
      5.2.2.9 Screen Copy ....................................................................................................................................................... 40
      5.2.2.10 Bit Set, Bit Reset ............................................................................................................................................... 41
   5.3 INITIALIZE ............................................................................................................................................................................. 42
   5.4 CHARACTER GENERATOR .................................................................................................................................................. 44
      5.4.1 Character Generator ROM ......................................................................................................................................... 44
      5.4.2 User Character Generator RAM ................................................................................................................................ 46
   5.5 ATTRIBUTE ........................................................................................................................................................................... 48
      5.5.1 Attribute Function ..................................................................................................................................................... 48
5.5.2 Procedure of setting attribute ....................................................................................................................... 49

6. APPLICATION CIRCUITS ..................................................................................................................................... 50
6.1 MODULE LOCATED IN THE MEMORY AREA OF CPU ....................................................................................... 50
6.2 MODULE LOCATED IN THE I/O AREA OF CPU ................................................................................................. 51
6.3 INTERFACE CIRCUIT WITH PPI LSI ............................................................................................................ 52

7. INSTALLATION ....................................................................................................................................................... 53

8. CAUTIONS AND HANDLING PRECAUTIONS ................................................................................................. 53
8.1 HANDLING ............................................................................................................................................................ 53
8.2 STORAGE ............................................................................................................................................................. 53
8.3 OPERATION .......................................................................................................................................................... 53
8.4 OTHERS ............................................................................................................................................................... 53

9. PROGRAM EXAMPLE ............................................................................................................................................ 54
1. Outline of LCD Module

The DMF 5000 series dot matrix graphic LCD modules include an LCD controller, a display RAM, a character generator ROM, and drive circuits. These modules are suitable for copiers, facsimiles, PBXs, marine instruments, and messaging displays for various instruments.

1.1 Features

1. Excellent readability and high contrast ratio.
2. Bit parallel bus interface.
3. Built-in LCD controller T6963C and display RAM (8K byte).
4. Large graphic display.
5. Various attribute functions.
6. Built-in 128 word character generator ROM, and 256 word (max.) character generator RAM.
7. Wide operating temperature range.
8. Compact and easily mountable on any equipment.
2. Specification

2.1 Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (Logic)</td>
<td>Vcc-Vss</td>
<td>-0.3</td>
<td>7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage (LCD Drive)</td>
<td>Vcc-Vee</td>
<td>Vcc +0.3</td>
<td>28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vcc-Vadj</td>
<td>0</td>
<td>28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>Vi</td>
<td>-0.3</td>
<td>Vcc +0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>Topr</td>
<td>0</td>
<td>+50</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Topr</td>
<td>+10</td>
<td>+40</td>
<td>°C</td>
<td>CCT Backlight Type</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>-20</td>
<td>+60</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

Make sure not to exceed above maximum rating values under the worst probable conditions.
### 2.2 Electrical Characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Standard Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
</tr>
<tr>
<td>Supply Voltage (Logic)</td>
<td>Vcc-Vss</td>
<td>Ta = 25° C</td>
<td>4.75</td>
<td>5</td>
</tr>
<tr>
<td>Supply Voltage (LCD Drive)</td>
<td>Vcc-Vee</td>
<td>Ta = 25° C</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage (LCD Drive)</td>
<td>Vcc-Vadj</td>
<td>Ta = 25° C</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td>Icc</td>
<td>Ta = 25° C</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Iee</td>
<td>Ta = 25° C</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Input Voltage “H” Level</td>
<td>ViH</td>
<td>Ta = 25° C</td>
<td>Vcc-2.2</td>
<td></td>
</tr>
<tr>
<td>Input Voltage “L” Level</td>
<td>ViL</td>
<td>Ta = 25° C</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
2.3 LCD Driving Voltage and Connection

The LCD Panel is driven by the voltage Vcc-Vee or Vcc-Vadj. Adjustable Vee or Vadj is required for contrast control and temperature compensation. Table 2.1 is a recommended power supply voltage for the LCD drive (Vcc-Vee or Vcc-Vadj).

<table>
<thead>
<tr>
<th>Model</th>
<th>Temp.</th>
<th>0 °C</th>
<th>10 °C</th>
<th>25 °C</th>
<th>40 °C</th>
<th>50 °C</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMF5001N Series</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1/128 Duty</td>
</tr>
<tr>
<td>(Vcc-Vadj)</td>
<td></td>
<td>23.2V</td>
<td></td>
<td>20.3V</td>
<td></td>
<td>18.3V</td>
<td></td>
</tr>
<tr>
<td>DMF5002N Series</td>
<td></td>
<td>22.4V</td>
<td></td>
<td>19.7V</td>
<td></td>
<td>17.6V</td>
<td>1/112 Duty</td>
</tr>
<tr>
<td>(Vcc-Vadj)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMF5003N Series</td>
<td></td>
<td>19.6V</td>
<td></td>
<td>18.4V</td>
<td></td>
<td>17.4V</td>
<td>1/128 Duty</td>
</tr>
<tr>
<td>(Vcc-Vadj)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CCTV Backlight</td>
</tr>
<tr>
<td>DMF5005N Series</td>
<td></td>
<td>14.8V</td>
<td></td>
<td>13.6V</td>
<td></td>
<td>12.3V</td>
<td>1/64 Duty</td>
</tr>
<tr>
<td>(Vcc-Vee)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMF5010N Series</td>
<td></td>
<td>14.4V</td>
<td></td>
<td>13.6V</td>
<td></td>
<td>12.8V</td>
<td>1/64 Duty</td>
</tr>
<tr>
<td>(Vcc-Vee)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CCTV Backlight</td>
</tr>
</tbody>
</table>

Consult your local Optrex representative to obtain detailed specifications for each module part number.
Example of power supply connection:

- +5V
- GND
- -12V

R: 5KΩ - 10KΩ
VR: 10KΩ - 20KΩ
Tr: 2SA, 1162Y etc.

Note: 

DMF5005N
DMF5010N Series

Vcc
Vss
Vee

DMF5001N
DMF5002N
DMF5003N Series

Vcc
Vss
Vee

Vadj
2.4 EL Back Light
Recommended Inverter and Connection

NEL-D32-49 Specification

Bottom View

Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>6VDC</td>
</tr>
<tr>
<td>Load (Lamp Surface Area)</td>
<td>95 cm²</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-20 - 70°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-10 - 55°C</td>
</tr>
</tbody>
</table>

Acceptable Operating Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>3-5.5VDC</td>
</tr>
<tr>
<td>Load (Lamp Surface Area)</td>
<td>50-83 cm²</td>
</tr>
</tbody>
</table>
2.5 CCT Back Light

Recommended Inverter and Connection

+24VDC VIN

CXA-1301 (TDK)

GND GND

DMF5003N
DMF5010N

OUT 1

GND

OUT 2

SERIES

CXA-1301 Specification

Bottom View

Maximum Ratings

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>26.4VDC</td>
</tr>
<tr>
<td>Output Power Consumption</td>
<td>5W</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-20 - 75 °C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>0 - 50 °C</td>
</tr>
</tbody>
</table>

Acceptable Operating Range

| Input Voltage | 24±1.2VDC |
3. Interface

3.1 Interface Connection

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Level</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FG</td>
<td>-</td>
<td>Frame Ground (Connected to Metal Holder)</td>
</tr>
<tr>
<td>2</td>
<td>VSS</td>
<td>-</td>
<td>Ground (Signal Ground)</td>
</tr>
<tr>
<td>3</td>
<td>VCC</td>
<td>-</td>
<td>Power Supply (Logic, LCD Drive)</td>
</tr>
<tr>
<td>4</td>
<td>VADJ</td>
<td>-</td>
<td>Power Supply for LCD Contrast Adjust</td>
</tr>
<tr>
<td>5</td>
<td>VEE</td>
<td>-</td>
<td>Power Supply (LCD Drive)</td>
</tr>
<tr>
<td>6</td>
<td>__</td>
<td>WR</td>
<td>Data Write (Write Data to the Module at “L”)</td>
</tr>
<tr>
<td>7</td>
<td>__</td>
<td>RD</td>
<td>Data Read (Read Data from the Module at “L”)</td>
</tr>
<tr>
<td>8</td>
<td>__</td>
<td>CE</td>
<td>Chip Enable for the Module</td>
</tr>
<tr>
<td>9</td>
<td>__</td>
<td>C/D</td>
<td>WR=“L”; C/D=“H”: Command Write, C/D=“L”: Data Write</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RD=“L”; C/D=“H”: Status Read, C/D=“L”: Data Read</td>
</tr>
<tr>
<td>10</td>
<td>__</td>
<td>HALT</td>
<td>L Stop the Oscillation of Clock</td>
</tr>
<tr>
<td>11</td>
<td>__</td>
<td>RESET</td>
<td>L Controller Reset</td>
</tr>
<tr>
<td>12</td>
<td>D6</td>
<td>H/L</td>
<td>Data Input/Output (LSB)</td>
</tr>
<tr>
<td>13</td>
<td>D1</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>14</td>
<td>D2</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>15</td>
<td>D3</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>16</td>
<td>D4</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>17</td>
<td>D5</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>18</td>
<td>D6</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>19</td>
<td>D7</td>
<td>H/L</td>
<td>Data Input/Output (MSB)</td>
</tr>
<tr>
<td>20</td>
<td>NC</td>
<td>-</td>
<td>No Connection</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Symbol</td>
<td>Level</td>
<td>Function</td>
</tr>
<tr>
<td>---------</td>
<td>--------</td>
<td>-------</td>
<td>----------</td>
</tr>
<tr>
<td>1</td>
<td>FG</td>
<td>-</td>
<td>Frame Ground (Connected to Metal Holder)</td>
</tr>
<tr>
<td>2</td>
<td>VSS</td>
<td>-</td>
<td>Ground (Signal Ground)</td>
</tr>
<tr>
<td>3</td>
<td>VCC</td>
<td>-</td>
<td>Power Supply (Logic, LCD Drive)</td>
</tr>
<tr>
<td>4</td>
<td>VEE</td>
<td>-</td>
<td>Power Supply (LCD Drive)</td>
</tr>
<tr>
<td>5</td>
<td>WR</td>
<td>L</td>
<td>Data Write (Write Data to the Module at “L”)</td>
</tr>
<tr>
<td>6</td>
<td>RD</td>
<td>L</td>
<td>Data Read (Read Data from the Module at “L”)</td>
</tr>
<tr>
<td>7</td>
<td>CE</td>
<td>L</td>
<td>Chip Enable for the Module</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td>-</td>
<td>No Connection</td>
</tr>
<tr>
<td>10</td>
<td>RESET</td>
<td>L</td>
<td>Controller Reset</td>
</tr>
<tr>
<td>11</td>
<td>Dφ</td>
<td>H/L</td>
<td>Data Input/Output (LSB)</td>
</tr>
<tr>
<td>12</td>
<td>D1</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>13</td>
<td>D2</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>14</td>
<td>D3</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>15</td>
<td>D4</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>16</td>
<td>D5</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>17</td>
<td>D6</td>
<td>H/L</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>18</td>
<td>D7</td>
<td>H/L</td>
<td>Data Input/Output (MSB)</td>
</tr>
<tr>
<td>19</td>
<td>FS</td>
<td>H/L</td>
<td>Font Size Select “H”: 6 x 8 DOT  “L”: 8 x 8 DOT</td>
</tr>
<tr>
<td>20</td>
<td>NC</td>
<td>-</td>
<td>No Connection</td>
</tr>
</tbody>
</table>
EL Back Light Terminal for DMF 5001N, 5002N, 5005N Series

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Level</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>EL</td>
<td>-</td>
<td>EL Power Supply</td>
</tr>
<tr>
<td>22</td>
<td>EL</td>
<td>-</td>
<td>EL Power Supply</td>
</tr>
</tbody>
</table>

CCT Back Light Terminal for DMF 5003N Series

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Level</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>-</td>
<td>Ground for CCT Power Supply</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>-</td>
<td>No Connection</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>-</td>
<td>No Connection</td>
</tr>
<tr>
<td>4</td>
<td>HOT</td>
<td>-</td>
<td>CCT Power Supply</td>
</tr>
</tbody>
</table>

CCT Back Light Terminal for DMF 5010N Series

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Level</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HOT</td>
<td>-</td>
<td>CCT Power Supply</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>-</td>
<td>No Connection</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>-</td>
<td>No Connection</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>-</td>
<td>Ground for CCT Power Supply</td>
</tr>
</tbody>
</table>
Pin No. Layout

DMF5001N, 5002N Series

Top View

1 2
19 20
21
22
EL

DMF 5003N Series

Top View

2 1
20

DMF 5005N Series

Top View

2 1
20
19

DMF 5010N Series

Top View

2 1
20
19

or

B4P-VH
or
B4PS-VH

JST

VHR-4N

CCT

EL

or

BP4-VH

BP4S-VH
3.2 Block Diagram

**NOTE**

*1: For DMF5001N, 5002N, 5003N series only.

*2: For DMF5005N, 5010N series only.

*3: DMF5003N, 5010N are already included.

*4: Available for DMF5001N, 5002N, 5005N
### 3.3 Signal Timings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>C/D Set Up Time</td>
<td>'CDS</td>
<td>100</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>C/D Hold Time</td>
<td>'CDH</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>CE, RD, WR Pulse Width</td>
<td>'CP, 'RP, 'WP</td>
<td>80</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data Set Up Time</td>
<td>'DS</td>
<td>80</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>'DH</td>
<td>40</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Access Time</td>
<td>'ACC</td>
<td>-</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>Output Hold Time</td>
<td>'OH</td>
<td>10</td>
<td>50</td>
<td>ns</td>
</tr>
</tbody>
</table>

Conditions: VCC = 5 ± 0.25V, GND = 0V, Ta = 25°C

![Bus Timing Diagram](image-url)
3.4 Memory Address and Display Position

[6 x 8 Font]

The relationship between display memory address and display position on the LCD module is defined in section 3.4.1. (note: this is for 6x8 character font)

Graphic home address GH, number of graphic area GA, text home address TH, and number of text area TA are defined by “Control Word Set” command. The position of GH, TH is described in 3.4.3 RAM map.

3.4.1 Memory Address and Display Position

Text Display (Ex. 240 x 64 DOT)

TA = 28H, GA = 28H
TH & GH = Within 0000H - 1FFFH

<table>
<thead>
<tr>
<th>TH</th>
<th>TH + 27H</th>
</tr>
</thead>
<tbody>
<tr>
<td>TH + TA</td>
<td>TH + TA + 27H</td>
</tr>
<tr>
<td>TH + 7TA</td>
<td>TH + 7TA + 27H</td>
</tr>
</tbody>
</table>

144444444444444424444444444444443
40 Character
Graphic Display (Ex. 240 x 64 DOT)

TA = 28H, GA = 28H  
TH & GH = Within 0000H - 1FFFH

<table>
<thead>
<tr>
<th>GH</th>
<th>GH + 27H</th>
</tr>
</thead>
<tbody>
<tr>
<td>GH + GA</td>
<td>GH + GA + 27H</td>
</tr>
<tr>
<td>GH + 63GA</td>
<td>GH + 63GA + 27H</td>
</tr>
</tbody>
</table>

64 Dot

14444444444444442444444444444444443  
40 x 6 = 240 Dot

Note: In case of graphic display, 8 bit data is as follows:

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>D6</td>
</tr>
<tr>
<td>1442443</td>
<td>14444444244444444443</td>
</tr>
<tr>
<td>Invalid Data</td>
<td>Valid Data</td>
</tr>
</tbody>
</table>
The relationship between display memory address and display position on the LCD module is defined in section 3.4.2. (note: this is for 8x8 character font)

Graphics home address GH, number of graphic area GA, text home address TH, and number of text area TA are defined by “Control Word Set” command. The position of GH, TH is described in 3.4.3 RAM map.

### 3.4.2 Memory Address and Display Position

**Text Display** (Ex. 240 x 64 DOT)

TA = 1EH, GA = 1EH  
TH & GH = Within 0000H – FFFH

<table>
<thead>
<tr>
<th>TH</th>
<th>TH + 1DH</th>
</tr>
</thead>
<tbody>
<tr>
<td>TH + TA</td>
<td>TH + TA + 1DH</td>
</tr>
<tr>
<td>TH + 7TA</td>
<td>TH + 7TA + 1DH</td>
</tr>
</tbody>
</table>

8 line

1444444444444444442444444444444444443  
30 Character
Graphic Display (Ex. 240 x 64 DOT)

TA = 1EH, GA = 1EH
TH & GH = Within 0000H ~ 1FFFH

<table>
<thead>
<tr>
<th>GH</th>
<th>TH + 1DH</th>
</tr>
</thead>
<tbody>
<tr>
<td>GH + GA</td>
<td>TH + TA + 1DH</td>
</tr>
<tr>
<td>GH + 63GA</td>
<td>TH + 7TA + 1DH</td>
</tr>
</tbody>
</table>

14444444444444442444444444444443
30 x 8 = 240 Dot

Note: In case of graphic display, 8 bit data is as follows:

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td>D6</td>
</tr>
<tr>
<td>D5</td>
<td>D4</td>
</tr>
<tr>
<td>D3</td>
<td>D2</td>
</tr>
<tr>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>

14444444444444442444444444444443
Valid Data
3.4.3 RAM Map

The Display RAM is built into the module, and display data is written to this display RAM. The built-in controller LSI/T6963C automatically reads the display RAM and sends the appropriate data to LCD drivers. The “Control Word Set” command (text home set, text area set, etc.) defines the RAM area which is read by the controller LSI making the RAM map programmable by the user. If more than 1 screen can be stored in the RAM. Vertical scrolling and paging is easily performed by resetting text home and/or graphic home address.

DMF5000 series have 8K byte built-in RAM located at address 0000H – 1FFFH, and the following is an example of RAM mapping (240 x 64 DOT).

- **Graphic RAM Area (0000H – 0EFFH)**
  - GH = 0000H
  - * 6 x 8 Font = 1.5 screen
  - * 8 x 8 Font = 2.0 screen
  - Text
  - For 256 characters

- **Attribute RAM Area (0F00H – 0FFFH)**

- **Text RAM Area (1000H – 1BFFH)**
  - TH = 1000H
  - * 6 x 8 Font = 9.6 screen
  - * 8 x 8 Font = 12.8 screen

- **C.G. RAM Area (1C00H – 1FFFH)**
  - CGRAM Offset register
  - For 128 words
  - Set data = “03H”
4. Soldering Jumper Setting

4.1 Initial Setting

Initial setting for “Font” and “Column” are described in Table 4.1.

<table>
<thead>
<tr>
<th>Series</th>
<th>Dot</th>
<th>Duty</th>
<th>Bias</th>
<th>Font</th>
<th>Column</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMF5001N Series</td>
<td>160 x 128</td>
<td>1/128</td>
<td>1/12</td>
<td>8 x 8</td>
<td>32 (valid 20)</td>
</tr>
<tr>
<td>DMF5002N Series</td>
<td>128 x 112</td>
<td>1/112</td>
<td>1/12</td>
<td>8 x 8</td>
<td>32 (valid 16)</td>
</tr>
<tr>
<td>DMF5003N Series</td>
<td>160 x 128</td>
<td>1/128</td>
<td>1/12</td>
<td>8 x 8</td>
<td>32 (valid 20)</td>
</tr>
<tr>
<td>DMF5005N Series</td>
<td>240 x 64</td>
<td>1/64</td>
<td>1/9</td>
<td>6 x 8 (FS=H)</td>
<td>64 (valid 40)</td>
</tr>
<tr>
<td>DMF5010N Series</td>
<td>240 x 64</td>
<td>1/64</td>
<td>1/9</td>
<td>6 x 8 (FS=H)</td>
<td>64 (valid 40)</td>
</tr>
</tbody>
</table>
4.2 Explanation of Each Soldering Jumper

* “Column” designate by soldering jumper.
  (J6, J7 for DMF5001N, 5002N, 5003N Series.
  J2, J3 for DMF5005N, 5010N Series.)

* “Character Font” designate by soldering jumper
  (J8, J9 for DMF5001N, 5002N, 5003N Series.
  F4, FS for DMF5005N 5010N Series.)

<table>
<thead>
<tr>
<th>DMF5001N, 5002N, 5003N Series</th>
<th>DMF5005N, 5010N Series</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Column</strong></td>
<td><strong>Column</strong></td>
</tr>
<tr>
<td></td>
<td>32 40 64 80</td>
</tr>
<tr>
<td>J6 H L H L</td>
<td>J2 H L H L</td>
</tr>
<tr>
<td>J7 H H L L</td>
<td>J3 H H L L</td>
</tr>
<tr>
<td>Initial set: J6, J7 = H</td>
<td>Initial set: J2 = H, J3 = L</td>
</tr>
</tbody>
</table>

| **Character Font**             | **Character Font**    |
| 5 x 8                          | 32 6 x 8 7 x 8 8 x 8 |
| J8 H L H L                     | J4 H L H L            |
| J9 H H L L                     | FS H H L L            |
| Initial set: J8, J9 = L        | Initial set: J4 = L, FS = Pull up (H) |

Note: 
H: +5V (Vcc) 
L: 0V (Vss) 
FS: I/O terminal pin no. 19 for designate the “Font” from outside of the module.
* Jumper Position

Note: All drawings are PWB's bottom view.
5. Communication between CPU and Module

5.1 Data Transmission Method

The built-in LCD controller, T6963C, is operating asynchronously to the CPU clock. The following procedure is required for data transmission between the module and the CPU.

(1) Command with 2 byte data

1. Status Read
2. NO
3. STA0=1, STA1=1
4. YES
5. Data Write D1 (lower 8 bit)
6. NO
7. STA0=1, STA1=1
8. YES
9. Data Write D2 (upper 8 bit)
10. NO
11. STA0=1, STA1=1
12. YES
13. Status Read
14. NO
15. STA0=1, STA1=1
16. Command Write

(2) Command with 1 byte data

1. Status Read
2. NO
3. STA0=1, STA1=1
4. YES
5. Data Write D1
6. Status Read
7. NO
8. STA0=1, STA1=1
9. YES
10. Command Write

(3) Command with no data

1. Status Read
2. NO
3. STA0=1, STA1=1
4. YES
5. Command Write
(4) Data Auto Write/Data Auto Read

STA2, STA3 should be checked between all data and command.
(Refer 5.2.2.6 “Data Auto Write/Data Auto Read”)

(5) Screen Peeking, Screen Copy

STA6 should be checked just after “Screen Peeking” / “Screen Copy”.
(Refer 5.2.2.8/9 “Screen Peeking”, “Screen Copy”)

5.1.1 Status Read

Status of the controller LSI should be checked between all command and data in order to complete a communication cycle with the CPU. The status can be read from 8 bit data lines (D0 to D7) by setting C/D=“H” and RD=“L”.

<table>
<thead>
<tr>
<th>STA0 (Busy1)</th>
<th>Check capability of instruction execution.</th>
<th>STA0=0 : Disable</th>
<th>STA0=1 : Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>STA1 (Busy2)</td>
<td>Check capability of data read or data write.</td>
<td>STA1=0 : Disable</td>
<td>STA1=1 : Enable</td>
</tr>
<tr>
<td>STA2 (DAV)</td>
<td>Check capability of data read (only effective in auto mode.)</td>
<td>STA2=0 : Disable</td>
<td>STA2=1 : Enable</td>
</tr>
<tr>
<td>STA3 (RDY)</td>
<td>Check capability of data write (only effective in auto mode.)</td>
<td>STA3=0 : Disable</td>
<td>STA3=1 : Enable</td>
</tr>
<tr>
<td>STA4</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>STA5 (CLR)</td>
<td>Check possibility of controller operation.</td>
<td>STA5=0 : Disable</td>
<td>STA5=1 : Enable</td>
</tr>
<tr>
<td>STA6 (Error)</td>
<td>Address pointer is out of graphic area on screen peeking and screen copy command.</td>
<td>STA6=1 : Out of graphic area</td>
<td></td>
</tr>
<tr>
<td>STA7 (Blink)</td>
<td>Check the condition of blink.</td>
<td>STA7=0 : Display off</td>
<td>STA7=1 : Normal display (on)</td>
</tr>
</tbody>
</table>

(Status Register)

<table>
<thead>
<tr>
<th>STA7</th>
<th>STA6</th>
<th>STA5</th>
<th>STA4</th>
<th>STA3</th>
<th>STA2</th>
<th>STA1</th>
<th>STA0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

|        |      |      |      |      |      |      |      |      |
| LSB    |      |      |      |      |      |      |      |      |
### 5.2 Command

#### 5.2.1 Command List

<table>
<thead>
<tr>
<th>Command</th>
<th>Command Code</th>
<th>Description</th>
<th>Execution Time (MAX) (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pointer Set</td>
<td>D7 D6 D5 D4 D3 D2 D1 D0</td>
<td>N2 N1 N0 0 0 1 Cursor pointer set 0 1 0 Offset register set 1 0 0 Address pointer set</td>
<td>Status Check</td>
</tr>
<tr>
<td>Control Word Set</td>
<td>0 1 0 0 0 0 N1 N0</td>
<td>N1 N0 0 0 Text home address set 0 1 Text area set 1 0 Graphic home address set 1 1 Graphic area set</td>
<td>Status Check</td>
</tr>
<tr>
<td>Mode Set</td>
<td>1 0 0 0 CG N2 N1 N0</td>
<td>CG=0: CG ROM Mode CG-1: CG RAM Mode N2 N1 N0 (Graphic and Text) 0 0 0 “OR” 0 0 1 “EXOR” 0 1 1 “AND” 1 0 0 Text only (attribute capability)</td>
<td>32x1/fOSC</td>
</tr>
<tr>
<td>Display Mode</td>
<td>1 0 0 1 N3 N2 N1 N0</td>
<td>N3=0: Graphic display off N2=0: Text display off N1=0: Cursor display off N0=0: Cursor blink off</td>
<td>32x1/fOSC</td>
</tr>
<tr>
<td>Cursor Pattern Select</td>
<td>1 0 1 0 0 N2 N1 N0</td>
<td>N2, N1, N0 specify the number of cursor lines. (EX) N2 N1 N0</td>
<td>32x1/fOSC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Command</td>
<td>Command Code</td>
<td>Description</td>
<td>Execution time (MAX) (Note 1)</td>
</tr>
<tr>
<td>-----------------------</td>
<td>--------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>-------------------------------</td>
</tr>
<tr>
<td></td>
<td>D7 D6 D5 D4 D3 D2 D1 D0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| Data Auto Read/Write  | 1 0 1 1 0 0 N1 N0 | N1 N0 Data auto write set  
0 0 Data auto write set  
0 1 Data auto read set  
1 * Auto reset  
After this command, continuous data can be written or read. (Address pointer automatically increment.) | 32x1/fOSC                     |
| Data Read/Write       | 1 1 0 0 0 N2 N1 N0 | Data read/write command for 1 byte.  
N2=0: Address pointer up/down  
=1: Address pointer unchanged  
N1=0: Address pointer up  
=1: Address pointer down  
N0=0: Data write  
=1: Data read |
| Screen Parking        | 1 1 1 0 0 0 0 0 | Transfer display data to data stack for read from CPU.                     | Status Check                  |
| Screen Copy           | 1 1 1 0 1 0 0 0 | 1 line displayed data which address is indicated by address pointer is copied to graphic RAM area. | Status Check                  |
| Bit Set/Reset         | 1 1 1 1 N3 N2 N1 N0 | Set/reset command for a bit in the address pointed by address pointer.  
N3=0: Bit reset  
=1: Bit set  
N2, N1, N0 indicate the bit in the pointed address. (000 is LSB, and 111 is MSB) | Status Check                  |

Note:
1. Status check between all commands and data is recommended, though execution time for several commands are specified in above command list.
For the commands with “status check” in execution time, execution time is not specified because it is variable depending on the internal operations of the controller LSI.

2. In case of 2 screen mode, Screen copy command cannot be used.
5.2.2 Description of Command

5.2.2.1 Pointer Set Command

<table>
<thead>
<tr>
<th>N2</th>
<th>N1</th>
<th>N0</th>
<th>Command</th>
<th>D1</th>
<th>D2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Cursor pointer set</td>
<td>Column position</td>
<td>Row Position</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Offset register set</td>
<td>Address</td>
<td>00H</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Address pointer set</td>
<td>Address (Lower)</td>
<td>Address (Upper)</td>
</tr>
</tbody>
</table>

(a) Cursor Pointer Set

The cursor is displayed at the position specified by the D1, D2. The cursor position is shifted only by this command, and does not shift by other commands. D1, D2 are specified as follows:

D1 : Horizontal cursor position counted by “character” (5 - 8 dot width/character specified by hard setting... refer 4 “Soldering Jumper Setting”). MSB of D1 is neglected, and 127 is the maximum.

D2 : Vertical cursor position counted by “character” (8 dot high character) (1st row of lower half screen is “11H”) Upper 3 bit are neglected and 32 is the maximum.

Note: Please note that the cursor position should be within actual display area.
(b) Offset Register Set

The offset register set command is used to determine the character generator RAM area. The upper 5 bits in start address of CG area is set as the lower 5 bits of D1, and the upper 3 bits of D1 are neglected. D2 should be 00H. Refer to section 5.4 “Character Generator” for details of the CG RAM.

(c) Address Pointer Set

The address pointer set command is used to indicate the start address for writing/reading data to/from the built-in RAM. The address should be located in the actual RAM area specified by individual specifications. (Refer to 3.4.3 “RAM MAP”.)

5.2.2.2 Control Word Set Command

D1, D2, 0 0 1 0 0 0 N1 N0

Home address of display RAM (Text, Graphic), and areas are defined by this command.

<table>
<thead>
<tr>
<th>N1</th>
<th>N0</th>
<th>Command</th>
<th>D1</th>
<th>D2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Text home address set (TH)</td>
<td>Address (Lower)</td>
<td>Address (Upper)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Text area set (TA)</td>
<td>No. of column</td>
<td>00H</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Graphic home address set (GH)</td>
<td>Address (Lower)</td>
<td>Address (Upper)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Graphic area set (GA)</td>
<td>No. of column</td>
<td>00H</td>
</tr>
</tbody>
</table>

(a) Text Home Address Set (TH)

This command defines the starting address of display RAM for text display. The data in the text home address (TH) is displayed at the home position of display (left end character on 1st row.)
(b) Text Area Set (TA)

This command defines the number of columns by D1. Text area can be defined independently from the number of characters fixed by hardware setting of controller LSI. The text area is usually defined as the actual number of characters on LCD display, so addressing can be continuous in the text area.

(c) Graphic Home Address Set (GH)

This command defines the starting address of display RAM for the graphic display. The data in the Graphic home address (GH) is displayed at the home position of display (left end 8 bits in 1st line). When using the attribute function, the graphic home address indicates the starting address of distribute RAM area.

(d) Graphic Address Set (GA)

This command defines the number of columns by D1. The graphic area can be defined independently from the number of characters fixed by hardware setting of controller LSI. If the graphic area is defined as the actual number of columns on the LCD display, the address in graphic area can be continuous and the RAM area can be used without ineffective areas. Note that the Graphic area will be different for depending on character font settings even if horizontal dot number is the same.

5.2.2.3 Mode Set Command

| (No data) | 1 | 0 | 0 | 0 | CG | N2 | N1 | N0 |

Mode set command selects character generator (CG ROM Mode/CG RAM Mode), and combination of text/graphic display.

<table>
<thead>
<tr>
<th>CG</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>CG ROM Mode: Built-in 128 character CG ROM (code: 00H - 7FH) and</td>
</tr>
<tr>
<td></td>
<td>built-in CG RAM for 128 characters can be used.</td>
</tr>
<tr>
<td>1</td>
<td>CG RAM Mode: Built-in CG RAM for 256 characters (code: 00H - FFH) can</td>
</tr>
<tr>
<td></td>
<td>be used.</td>
</tr>
</tbody>
</table>
When CG ROM Mode is selected, character code 00H - 7FH is selected from built-in CG ROM and 80H - FFH is automatically selected from CG RAM.

<table>
<thead>
<tr>
<th>N2</th>
<th>N1</th>
<th>N0</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Logically “OR” of Graphic and Text display.</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Logically “EXOR” of Graphic and Text display.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Logically “AND” of Graphic and Text display.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Text display only (text can be attributed by the data in the graphic area.)</td>
</tr>
</tbody>
</table>

Logically “OR”, “EXOR”, and “AND” of graphic and text display can be displayed by this command. Only text display is attributed because Attribute RAM is located in Graphic RAM area. (Refer 5.5 “Attribute”)

### 5.2.2.4 Display Mode Set Command

<table>
<thead>
<tr>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>N0</td>
</tr>
<tr>
<td>N1</td>
</tr>
<tr>
<td>N2</td>
</tr>
<tr>
<td>N3</td>
</tr>
</tbody>
</table>

Display mode is selected from combination of following 4 bits by setting “1” at the selected bit.

After hard reset, all displays are inhibited. (N0=N1=N2=N3=0)
### 5.2.2.5 Cursor Pattern Select Command

When cursor display is “ON”, this command selects the cursor pattern from 1 line width cursor to 8 line width cursor (block).

<table>
<thead>
<tr>
<th>N2</th>
<th>N1</th>
<th>N0</th>
<th>Cursor pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1 line width cursor</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>2 line width cursor</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>3 line width cursor</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>4 line width cursor</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5 line width cursor</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>6 line width cursor</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>7 line width cursor</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8 line width cursor</td>
</tr>
</tbody>
</table>

(1 line width cursor)

(8 line width cursor)
<table>
<thead>
<tr>
<th>N1</th>
<th>N0</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Data Auto Write Set</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Data Auto Read Set</td>
</tr>
<tr>
<td>1</td>
<td>*</td>
<td>Auto Mode Reset</td>
</tr>
</tbody>
</table>

*: Don’t care.

Note: Status check for auto mode (STA2, STA3) should be checked between each data. Auto reset should be performed after checking STA3=1 (Data Auto Write only). Refer to the following chart.
5.2.2.7 Data Write/Data Read

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>N2</th>
<th>N1</th>
<th>N0</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: D1 is necessary only for data write.

This command is used for data write from CPU to built-in RAM, and data read from built-in RAM to CPU. Data write/data read should be executed after setting address by address pointer set command. Address pointer can be automatically increment or decrement by setting this command.

<table>
<thead>
<tr>
<th>N2</th>
<th>N1</th>
<th>N0</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Data Write (after execution address pointer increment)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Data Read (after execution address pointer increment)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Data Write (after execution address pointer decrement)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Data Read (after execution address pointer decrement)</td>
</tr>
<tr>
<td>1</td>
<td>*</td>
<td>0</td>
<td>Data Write (after execution address pointer unchanged)</td>
</tr>
<tr>
<td>1</td>
<td>*</td>
<td>1</td>
<td>Data Read (after execution address pointer unchanged)</td>
</tr>
</tbody>
</table>

*: Don’t care

This command is necessary for each 1 byte data.

5.2.2.8 Screen Parking

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>(No data)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This command is used to transfer displayed 1 byte data to data stack, and this 1 byte data can be read from CPU by data read command. So, logical combination data of text and graphic display on LCD screen can be read by this command. Status (STA6) should be checked just after “screen peeking” command. If the address determined by “address pointer set” command is not in graphic RAM area, this command is ignored and status flag (STA6) is set.
The procedure to read displayed data using this command is as follows:

Screen peeking command can be used for getting hard copy of LCD display. Another application of this command is that modified CG is set in the CG RAM area by reading combination data of text and graphic data and writing to CG RAM area. For example, CG for reverse character is made by this method.
5.2.2.9  Screen Copy

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
</tr>
</thead>
</table>

1 low data displayed in LCD screen can be copied to the graphic RAM area specified by “address pointer set” command. Start point of 1 low data in the screen is determined by the “address pointer set” command. If attribute for text display is set by "Mode Set" command, “screen copy” command cannot be used.

Status (STA6) should be checked just after this command. If the address determined by “address pointer set” command is not located in graphic RAM area, this command is ignored and status flag (STA6) is set. The procedure to copy the displayed data using this command is as follows.

Note: In case of 2 screen mode, Screen copy command cannot be used.
5.2.2.10 Bit Set, Bit Reset

<table>
<thead>
<tr>
<th></th>
<th>N3</th>
<th>N2</th>
<th>N1</th>
<th>N0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>N3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N0</td>
</tr>
</tbody>
</table>

One bit in the 1 byte data specified by “address pointer set” command can be set or reset. Plural bits in the 1 byte data cannot be set/reset at a time.

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>N3 = 1 : bit set, N3 = 0 : bit reset</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>N2</th>
<th>N1</th>
<th>N0</th>
</tr>
</thead>
<tbody>
<tr>
<td>N2, N1, N0 specify the bit for set/reset.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
## 5.3 Initialize

Initialize of controller LSI T6963C is required for “Mode set”, “Control word set” after power on. Following is the one example of initialize procedure of 240 x 64 dot display.

<table>
<thead>
<tr>
<th>Command</th>
<th>C/D</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power on</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hard reset (Use reset terminal)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RESET=“L” (lmSec minimum after Vcc ≥ 4.75V)</td>
</tr>
<tr>
<td>Mode set</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>“OR” mode</td>
</tr>
<tr>
<td>Control word set</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Graphic home position set</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Graphic home address command</td>
</tr>
<tr>
<td>(Graphic home position 0000H)</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Number of graphic area set</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Number of area Command</td>
</tr>
<tr>
<td>(Graphic 30 x 8 dots)</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Text home position set</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Text home position 1000H)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Text home address</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Command</td>
</tr>
<tr>
<td>Number of text area set</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Text 30 column)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Number of area Command</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>(Initialize end)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Data write)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address pointer set</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Graphic home address</td>
</tr>
<tr>
<td>(Address pointer 0000H)</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Command</td>
</tr>
<tr>
<td>Data write (Graphic)</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Data Command</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Data Command</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Address pointer set</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Text home address</td>
</tr>
<tr>
<td>(Address pointer 1000H)</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Command</td>
</tr>
<tr>
<td>Data write (Text)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Data Command</td>
</tr>
<tr>
<td>(o)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Data Command</td>
</tr>
<tr>
<td>(p)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Display Mode Set</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(Text/Graphic on)</td>
</tr>
</tbody>
</table>

Note:

1. “Status check” should be inserted between all command and data.
Display mode set register is cleared (no display mode) by the hard reset, and no display is appeared on LCD panel. And just after “Display Mode set 9CH”, written data is displayed on the LCD.
5.4 **Character Generator**

5.4.1 **Character Generator ROM**
Character generator ROM for 128 characters is built-in this module.

**Character code map**

ROM Code 0101

<table>
<thead>
<tr>
<th>ASO</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td><img src="image1.png" alt="Character Codes" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td><img src="image2.png" alt="Character Codes" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td><img src="image3.png" alt="Character Codes" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td><img src="image4.png" alt="Character Codes" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td><img src="image5.png" alt="Character Codes" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td><img src="image6.png" alt="Character Codes" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td><img src="image7.png" alt="Character Codes" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td><img src="image8.png" alt="Character Codes" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.4.2 User Character Generator RAM

The character generator RAM is the built-in RAM which can be used as character generator after writing character pattern by program. The part of built-in RAM can be used as “User CG RAM” for 256 characters by selecting “CG RAM Mode”, or for 128 characters by selecting “CG ROM Mode”.

1) Position of User CG RAM

The upper 5 bits in start address of User CG RAM (NNNNN) is defined by “Pointer Set” command (Offset register set), and following 2048 byte are defined as “User CG RAM” area when CG RAM Mode is selected. 1024 byte (address: NNNNN10000000000 - NNNNN11111111111) is defined as “User CG RAM” area when CG ROM Mode is selected.

2) Writing to User CG RAM

Character pattern of specified CG code can be written in the pointed address by “Pointer Set” command (Address pointer set). 8 byte data should be sent to following 8 byte address for 1 character.

```
(MSB)         (LSB)
N N N N N M * * * * * * * * * *
```

Upper 5 bit defined by CG code (8 bit) Automatically
“pointer Set” command M=1 for CG ROM Mode scan for display
(Offset register set) M=0 for CG RAM Mode

3) Display Pattern in User CG RAM

Character pattern can be displayed by sending CG code with “Data Write” command. But “Display Mode Set” for text display should be selected before using CG. In case that “CG ROM Mode” is selected, character pattern is selected from built-in CG ROM when MSB=1 (00H - 7FH), and from User CG RAM when MSB=0 (80H-FFH). In case that “CG RM Mode” is selected, all character patterns are selected from User CG RAM (00H-FFH).
4) Relation between User CG RAM Address and CG code and Character Pattern.

When character pattern is written to User CG RAM, relation between CG code and “User CG RAM” address is shown in the following chart:

<table>
<thead>
<tr>
<th>Character Code</th>
<th>RAM Address for User CG</th>
<th>Character Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>M 0 0 0 0 0 0</td>
<td>N N N N M 0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>M 0 0 0 0 0 1</td>
<td>N N N N M 0 0 0 0 0 1 0</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>M 0 0 0 0 1 0</td>
<td>N N N N M 0 0 0 0 1 0 0</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1 1 1 1 1 1</td>
<td>N N N N 1 1 1 1 1 1 1 1 0</td>
<td>0 1 1 1 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>

Note 1:

Character code in “User CG RAM” is located from 80H to FFH in case of “CG ROM Mode”, and from 00H to FFH in case of “CG RAM Mode”. So, M in above chart is as follows:

M=1 : “CG ROM Mode”
M=0 : “CG RAM Mode”
Note 2:

“NNNNN” is the upper 5 bits in start address of User CG RAM defined by “Pointer Set” command (Offset Register Set).

Note 3:

It must be careful so that User CG RAM area should not be rewritten by display data, etc.

5.5 Attribute

5.5.1 Attribute Function

This module has attribute function for “Reverse display”, “Blink” in text display mode. Attribute data is written in the “Graphic area” defined by “Control word set” command (Graphic home address set and Graphic area set). So “Text display only” Mode should be selected by “Mode Set” command, and graphic display cannot be displayed.

The attribute data of the 1st character in “Text area” is written at the 1st byte in “graphic area”, and attribute data of nth character is written at the nth 1 byte in “Graphic area”. Attribute function is defined as follows:

Attribute RAM

<table>
<thead>
<tr>
<th>N3</th>
<th>N2</th>
<th>N1</th>
<th>N0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Normal display</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Reverse display (Text only)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Inhibit display</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Blink of normal display</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Blink of reverse display</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Inhibit display</td>
</tr>
</tbody>
</table>

*: Don’t care
### 5.5.2 Procedure of setting attribute

The example of the procedure of setting attribute is as follows:

<table>
<thead>
<tr>
<th>Command</th>
<th>C/D</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Graphic display off</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
</tr>
<tr>
<td>Graphic address home set</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>home address 1400H</td>
</tr>
<tr>
<td>Attribute data write</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Mode set</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Graphic display on</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>*</td>
<td>*</td>
<td></td>
</tr>
</tbody>
</table>

* : Don’t care
6. Application Circuits

Following diagrams are the examples of interface circuit with CPU TMPZ84C00P (Z80, CMOS 4MHz). For the interface to 16 bit CPU, please refer the diagram using PPI LSI (TMP82C55).

6.1 Module Located in the Memory Area of CPU

The module can be directly connected to CPU data bus as following diagram. Control signals of the module are made from MREQ, WR, RD signals of CPU, and chip select signal from address decoder. LSB of address bus (A0) can be used as C/D (command/data selection) signal.
6.2 Module Located in the I/O Area of CPU

The module can be controlled as the device located in the I/O area. Control signals are made from IORQ, WR, RD of CPU, and the chop select signal from address decoder. LSB of address bus (A0) can be used as C/D (command/data selection) signal.
6.3 Interface Circuit with PPI LSI

The module can be interfaced with PPI LSI as shown in the following diagram. 8 bit data bus of the module is connected to A port of PPI, and control signals C/D, CE, WR, RD) are sent from upper 4 bit of C port. In following diagram PPI is located in the I/O address area, but interface between CPU and PPI can be left for user’s design.

[Diagram of the interface circuit]
7. Installation
For installation of the module, please use four mounting holes located at the corners of PCB or Bezel. The Bezel is not intended to be used as a cosmetic purpose. A proper protective cover (lens) over the LCD surface and a proper enclosure are recommended to be used in order to prevent LCD surface (polarizer) from scratching or staining.

8. Cautions and Handling Precautions

8.1 Handling
a) Refrain from strong mechanical shock or applying force to the display plane. It may cause malfunction or damage of LCD.
b) In the case of leakage of liquid crystal material, avoid ingestion, contact of skin. If liquid crystal material sticks to skin, wash with alcohol and rinse thoroughly with water.
c) Note that LCD surface (polarizer) is very soft as is easily damaged. Do not press the polarizer surface with hard object.
d) The polarizer and adhesive used for lamination may be attacked by some organic solvent. When LCD surface becomes dirty wipe softly with absorbent cotton soaked in benzene.
e) Protect the LCD module from the electro-static discharge. It will damage C-MOS LSI in the module.

8.2 Storage
a) Do not leave the LCD module in high temperature, especially in high humidity for a long time. It is recommended to store it in the place where the temperature is between 0°C and 35°C, and where the humidity is lower than 70%.
b) Store the module without exposure to the direct sunlight.

8.3 Operation
a) Do not connect or remove LCD module to main system with power applied.
b) Power supplies should always be turned on before the independent input signal sources are turned on, and input signals should be turned off before power supplies are turned off.

8.4 Others
a) Avoid condensation of water, it may cause mis-operation or corrosion of electrode.
b) Ultraviolet ray cut filter is necessary for outdoor operation.
c) Do not exceed the maximum ratings under the worst probable conditions with respect to supply voltage variation, input voltage variation, environmental temperature, etc.
9. Program Example

DMF-5001 DEMO 87.9.21
MACRO-80 3.4 01-Dec-80 Page 1

TITLE DMF-5001 DEMO 87.9.21
; ####################################################################
; ###        ###
; ### DMF-5001 DEMO MACHINE ###
; ### VER. 1.0 ###
; ### 1987.9.26 ###
; ###        ###
; ####################################################################
; PROGRAM NAME : D5001.MAC
;
.Z80
0000   ASEG
       ORG 0
0000   PA EQU 0
0001   PB EQU 1
0002   PC EQU 2
0003   CW EQU 3
0010   LCD EQU 10H
8800   STACK EQU 8800H
2000   DATA1 EQU 2000H
4000   DATA2 EQU 4000H
6000   DATA3 EQU 6000H
A000   DATA4 EQU 0A000H
;
0000   F3   DI
0001   31 8800   LD SP, STACK
; 8255 MODE SET
0004   3E 82   LD A,82H
0006   D3 03   OUT (CW),A
;
0008   3E 80   LD A,80H
000A   CD 016C CALL CWRT
; ---------------------------------------------------------
; ============================
; MAIN ROUTINE
; ============================
000D   MAIN:
000D   CD 00DA CALL TMST ; TEXT MODE SET
0010   21 2000 LD HL,DATA1
0013   01 0140 LD BC,16*20
0016   MAIN10:
0016   CD 0156 CALL SAREAD
0019   7E   LD A,(HL)
001A   D6 20 SUB 20H
001C CD 0178 CALL DWRT
001F  23 INC HL
0020  OB DEC BC
0021  78 LD A,B
0022  B1 OR C
0023  C2 0016 JP NZ,MAIN10
0026  21 4000 LD HL,DATA2
0029  01 0140 LD BC,16*20

DMF-5001 DEMO 87.9.21 MACRO-80 3.4 01-Dec-80 Page 1-1

002C MAIN11:
002C CD 0156 CALL SAREAD
002F  7E LD A,(HL)
0030  D6 20 SUB 20H
0032  CD 0178 CALL DWRT
0035  23 INC HL
0036  OB DEC BC
0037  78 LD A,B
0038  B1 OR C
0039  C2 002C JP NZ,MAIN11

; 003C 21 6000 LD HL,DATA3
003F  01 0140 LD BC,16*20
0042 MAIN12:
0042 CD 0156 CALL SAREAD
0045  7E LD A,(HL)
0046  D6 20 SUB 20H
0048  CD 0178 CALL DWRT
004B  23 INC HL
004C  0B DEC BC
004D  78 LD A,B
004E  B1 OR C
004F  C2 0042 JP NZ,MAIN12

; 0052 3E B2 LD A.0B2H
0054  CD 016C CALL CWRT ; AUTO WRITE RESET

; 0057 CD 010D CALL GMSET
005A  21 A000 LD HL,DATA4
005D  01 A000 LD BC,16*20*8
0060 MAIN13:
0060 CD 0156 CALL SAREAD
0063  7E LD A,(HL)
0064  CD 01A4 CALL BCG ; DATA CHANGE
0067  CD 0178 CALL DWRT
006A  23 INC HL
006B  0B DEC BC
0063  78     LD   A,B
006D B1 OR    C
006E C2 0060 JP    NZ,MAIN13

0071  3E B2 LD    A,0B2H
0073 CD 016C CALL   CWRT          ; AUTO WRITE RESET

0076  16 00 LD    D,0          ; COUNTER RESET
0078 MAIN50:
0078  7A LD    A,D
0079 FE 00 CP    0
007B C2 0084 JP    NZ,MAIN51
007E 21 0000 LD    HL,0000H  ; DATA1 START
0081 C3 00A4 JP    MAIN60
0084 MAIN51:
0084  FE 01 CP    1
0086 C2 008F JP    NZ,MAIN52
0089 21 0140 LD    HL,0140H  ; DATA2 START
008C C3 00A4 JP    MAIN60

DMF-5001 DEMO 87.9.21   MACRO-80 3.4 01-Dec-80 Page 1-2

008F MAIN52:
008F  FE 02 CP    2
0091 C2 009A JP    NZ,MAIN53
0094 21 0280 LD    HL,0280H  ; DATA3 START
0097 C3 00A4 JP    MAIN60
009A MAIN53:
009A  3E 98 LD    A,98H
009C CD 016C CALL   CWRT
009F  16 00 LD    D,0
00A1 C3 00BA JP    MAIN20
00A4 MAIN60:
00A4  7D LD    A,L
00A5 CD 0178 CALL   DWRT
00A8  7C LD    A,H
00A9 CD 0178 CALL   DWRT
00AC  3E 40 LD    A,40H          ; TEXT HOME ADDRESS
00AE CD 016C CALL   CWRT

00B1 3E 94 LD    A,94H          ; TEXT ON
00B3 CD 016C CALL   CWRT
00B6 14 INC    D
00B7 C3 00BA JP    MAIN20

; -----------------------------------------------------------------------------
; SWITCH CHECK LOOP
; -----------------------------------------------------------------------------

00BA MAIN20:
00BA CD 0199 CALL   SWOFF
MAIN30:
0FBD  0E 01    LD    C,PB
0FBF CD 01E2    CALL  INPUT
0FC2 CB 47    BIT   0,A
0FC4 C2 00D1    JP    NZ,MAIN40
0FC7 CD 018A    CALL  SWON ; SW ON CHECK
0FCA  B7 OR A
0FCB  CA 00 78    JP   Z,MAIN50 ; NEXT MODE
0FCE C3 00BD    JP    MAIN30

MAIN40:
0FCD 9C40    LD    BC,40000
0FDF CD 01F4    CALL  DELAY
0FD7 C3 0078    JP    MAIN50

; -------------------------------------------------------------
; TMSET: TEXT MODE SET
; -------------------------------------------------------------
0FDA    TMSET:
0FDB 3E 00    LD    A,0 ; D1
0FDC CD 0178    CALL  DWRT

; 0FDE 3E 00    LD    A,0 ; D2
0FEC CD 0178    CALL  DWRT

; 0FEE 3E 40    LD    A,40H ; TEXT HOME ADRS
0FED CD 016C    CALL  CWRT

; --------------------------------------------------------------
0FE9 3E 14    LD    A,14H ; D1 20

DMF-5001 DEMO 87.9.21  MACRO-80 3.4  01-Dec-80 Page 1-3
0FEB CD 0178    CALL  DWRT

; 0FEE 3E 00    LD    A,0 ; D2
0FEC CD 0178    CALL  DWRT

; 0FED 3E 41    LD    A,41H ; AREA SET
0FEE CD 016C    CALL  CWRT

; --------------------------------------------------------------
0FF8 3E 00    LD    A,0 ; D1
0FFA CD 0178    CALL  DWRT

; 0FFD 3E 00    LD    A,0 ; D2
0FFF CD 0178    CALL  DWRT

; 0102 3E 00    LD    A,0 ; D2
0104 CD 016C    CALL  CWRT

; --------------------------------------------------------------
0107 3E B0    LD    A,0B0H ; AUTO WRITE SET
0109 CD 016C CALL CWRT
010C C9 RET

; ----------------------------------------------------------------
; GMSET : GRAPHIC MODE SET
; ----------------------------------------------------------------

010D GMSET:
010D 3E 00 LD A,0 ; D1
010F CD 0178 CALL DWRT

; 0112 3E 05 LD A,05H ; D2
0114 CD 0178 CALL DWRT
;
0117 3E 42 LD A,42H ; GRAPHIC HOME ADRS
0119 CD 016C CALL CWRT

; ----------------------------------------------------------------
011C 3E 14 LD A,14H ; D1 20
011E CD 0178 CALL DWRT
;
0121 3E 00 LD A,0 ; D2
0123 CD 0178 CALL DWRT
;
0126 3E 43 LD A,43H ; AREA SET
0128 CD 016C CALL CWRT

; ----------------------------------------------------------------
012B 3E 00 LD A,0 ; D1
012D CD 0178 CALL DWRT
;
0130 3E 05 LD A,05H ; D2
0132 CD 0178 CALL DWRT
;
0135 3E 24 LD A,24H ; ADDRESS POINT SET
0137 CD 016C CALL CWRT

; ----------------------------------------------------------------
013A 3E B0 LD A,0B0H ; AUTO WRITE SET
013C CD 016C CALL CWRT
013F C9 RET

; -----------------------------------------------------------------
DMF-5001 DEMO 87.9.21 MACRO-80 3.4 01-Dec-80 Page 1-4

; SREAD: STATAS READ
; -----------------------------------------------------------------
0140 SREAD:
0140 F5 PUSH AF
0141 C5 PUSH BC
0142 D5 PUSH DE
0143 E5 PUSH HL
C0 0144 3E 01  LD     A,1
C0 0146  D3 00  OUT    (PA),A
C0 0148   SRD00:
C0 0148  DB 10  IN      A,(LCD)
C0 014A  E6 03  AND    3
C0 014C  FE 03  CP      3
C0 014E  C2 0148  JP     NZ,SRD00

    ;
C0 0151  E1    POP     HL
C0 0152  D1    POP     DE
C0 0153  C1    POP     BC
C0 0154  F1    POP     AF
C0 0155  C9    RET
C0 0156   SREAD:
C0 0156  F5    PUSH    AF
C0 0157  C5    PUSH    BC
C0 0158  D5    PUSH    DE
C0 0159  E5    PUSH    HL

    ;
C0 015A 3E 01  LD     A,1
C0 015C  D3 00  OUT    (PA),A
C0 015E   SARD0:
C0 015E  DB 10  IN      A,(LCD)
C0 0160  E6 08  AND    8
C0 0162  FE 08  CP      8
C0 0164  C2 015E  JP     NZ,SARD0

    ;
C0 0167  E1    POP     HL
C0 0168  D1    POP     DE
C0 0169  C1    POP     BC
C0 016A  F1    POP     AF
C0 016B  C9    RET

    ;

;--------------------------------------------------------
;  CWRT: COMMAND WRITE
;--------------------------------------------------------

C0 016C  C0140  CALL    SREAD
C0 016F  F5    PUSH    AF
C0 170 3E 01  LD     A,1
C0 0172  D3 00  OUT    (PA),A
C0 0174  F1    POP     AF
C0 0175  D3 10  OUT    (LCD),A
C0 0177  C9    RET

    ;

;--------------------------------------------------------
;  DWRT: DATA WRITE
;--------------------------------------------------------
0178    DWRT:
0178    CD 0140    CALL  SREAD
017B    DWRT0:
017B F5    PUSH  AF
017C 3E 00    LD   A,0
017E D3 00    OUT  (PA),A
0180    D3 10    OUT  (LCD),A
0183    C9     RET

0184    DWRT2:
0184    CD 0156    CALL  SAREAD
0187    C3 017B    JP   DWRT0

; ----------------------------------------------------------
;  SWON:  MANUAL SW ON CHECK
; ----------------------------------------------------------
018A    SWON:
018A    0E 01    LD   C,PB
018C    CD 01E2    CALL  INPUT
018F    CB 4F    BIT  1,A
0191    CA 0197    JP   Z,SWON0
0194    3E FF    LD   A,0FFH
0196    CF     RET
0197    SWON0:
0197    AF     XOR  A
0198    C9     RET

; ----------------------------------------------------------
;  SWOFF:  MANUAL SW OFF CHECK
; ----------------------------------------------------------
0199    SWOFF:
0199    0E 01    LD   C,PB
019B    CD 01E2    CALL  INPUT
019E    CD 4F    BIT  1,A
019F    CA 0199    JP   Z,SWOFF
01A3    C9     RET

; ----------------------------------------------------------
;  BIT CHANGE
; ----------------------------------------------------------
01A4    BCG:
01A4    C5     PUSH  BC
01A5    06 00    LD   B,0
01A7    CB 47    BO:  BIT  0,A
01A9    CA 01AE    JP   Z,B1
01AC    CB F8    SET  7,B
01AE    CB 4F    B1:  BIT  1,A
01B0    CA 01B5    JP   Z,B2
01B3    CB F0    SET  6,B
01B5    CB 57    B2:  BIT  2,A
01B7 CA 01BC JP Z.B3
01BA CB E8 SET 5B
01BC CB 5F BIT 3,A
01BE CA 01C3 B3: JP Z.B4
01C1 CB E0 SET 4.B
01C3 CB 67 B4: BIT 4.A
01C5 CA 01CA JP Z.B5

DMF-5001 DEMO 87.9.21 MACRO-80 3.4 01-Dec-80 Page 1-6

01C8 CB D8 SET 3.B
01CA CB 6F B5: BIT 5.A
01CC CA 01D1 JP Z.B6
01CF CB D0 SET 2.B
01D1 CB 77 B6: BIT 6.A
01D3 CA 01D8 JP Z.B7
01D6 CB C8 SET 1.B
01D8 CB 7F B7: BIT 7.A
01DA CA 01DF JP Z.B8
01DD CB C0 SET 0.B
01DF B8:
01DF 78 LD A,B
01E0 C8 POP BC
01E1 C9 RET

;-------------------------------------------------------------
; INPUT: C: PORT ADDRESS
;-------------------------------------------------------------
01E2 C5 PBBC
01E3 D5 PBDE
01E4 INPUT1:
01E4 06 01 LD B,10
01E6 ED 78 IN A.(C)
01E8 57 LD D.A
01E9 INPUT2:
01E9 ED 78 IN A.(C)
01EB BA CP D
01EC C2 01E4 JP NZ,INPUT1
01EF 10 F8 DJNZ INPUT2
01F1 D1 POP DE
01F2 C1 POP BC
01F3 C9 RET

;-------------------------------------------------------------
; DELAY: BC LOOP CNT
; (171*BC+44)*.25*10^-6 (SEC)
;-------------------------------------------------------------
01F4 C5 PBBC
01F5 D5 PBDE
01F6 1E10 DEL1: LD E,10H
01F8 1D DEL2: DEC E
01F9 C2 01F8 JP NZ,DEL2
01FC 0B DEC BC
01FD 78 LD A,B
01FF C2 01F6 JP NZ,DEL1
0202 D1 POP DE
0203 C1 POP BC
0204 C9 RET
0205 00 00 00 00 DEFB 0,0,0,0
END

DMF-5001 DEMO 87.9.21 MACRO-80 3.4 01-Dec-80 Page S

Macros:

Symbols:

B0 01A7 B1 01AE B2 01B5 B3 01BC
B4 01C3 B5 01CA B6 01D1 B7 01D8
B8 01DF BCG 01A4 CW 0003 CWRT 016C
DATA1 2000 DAT2 4000 DATA3 6000 DATA4 A000
DEL1 0AF6 DEL2 01F8 DELAY 01F4 DWRT 0178
DWRT0 017B DWRT2 0184 GMSET 010D INPUT 01E2
INPUT1 01E4 INPUT2 01E9 LCD 0010 MAIN 000D
MAIN10 0016 MAIN11 002C MAIN12 0042 MAIN13 0060
MAIN20 00BA MAIN30 00BD MAIN40 00D1 MAIN50 0078
MAIN51 0084 MAIN52 008F MAIN53 009A MAIN60 00A4
PA 0000 PB 0001 PC 0002 SARD0 015E
SAREAD 0156 SREAD 0148 SREAD 0140 STACK 8800
SWOFF 0156 SWON 018A SWON0 0197 TMSET 00DA

No Fatal error(s)