



**NOVATEK**  
聯詠科技

# *Data Sheet*

***NT7534***

132 X 65 RAM-Map STN LCD

Controller/Driver

***V1.0***

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**Revision History**

<b>NT7534 Specification Revision History</b>		
<b>Version</b>	<b>Content</b>	<b>Date</b>
1.0	Released	Dec. 2004

## Features

- 132 x 65-dot graphics display LCD controller/driver for black/white STN LCD
- RAM capacity: 132 x 65 = 8,580 bits
- 8-bit parallel bus interface for both 8080 and 6800 series, 4-wire Serial Peripheral Interface (SPI)
- Direct RAM data display using the display data RAM.  
When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed.  
(At normal display)
- Many command functions:  
Read/Write display data, display ON/OFF, Normal/Reverse display, page address set, display start line set, LCD bias set, electronic contrast controls, V0 voltage regulation internal resistor ratio set, read modify write, segment driver direction select, power save.
- Other command functions:  
Partial display, partial start line set, N-Line inversion.
- Power supply voltage:
  - VDD = 1.8 ~ 3.6 V
  - VDD2 = 1.8 ~ 3.6 V
  - V0 = 4.0 ~ 14.2 V
  - VOUT = 14.2 V Max.
- 2X / 3X / 4X / 5X on chip DC-DC converter
- On chip LCD driving voltage generator or external power supply selectable
- 64-step contrast adjuster and on chip voltage follower
- On chip oscillation and hardware reset

## General Description

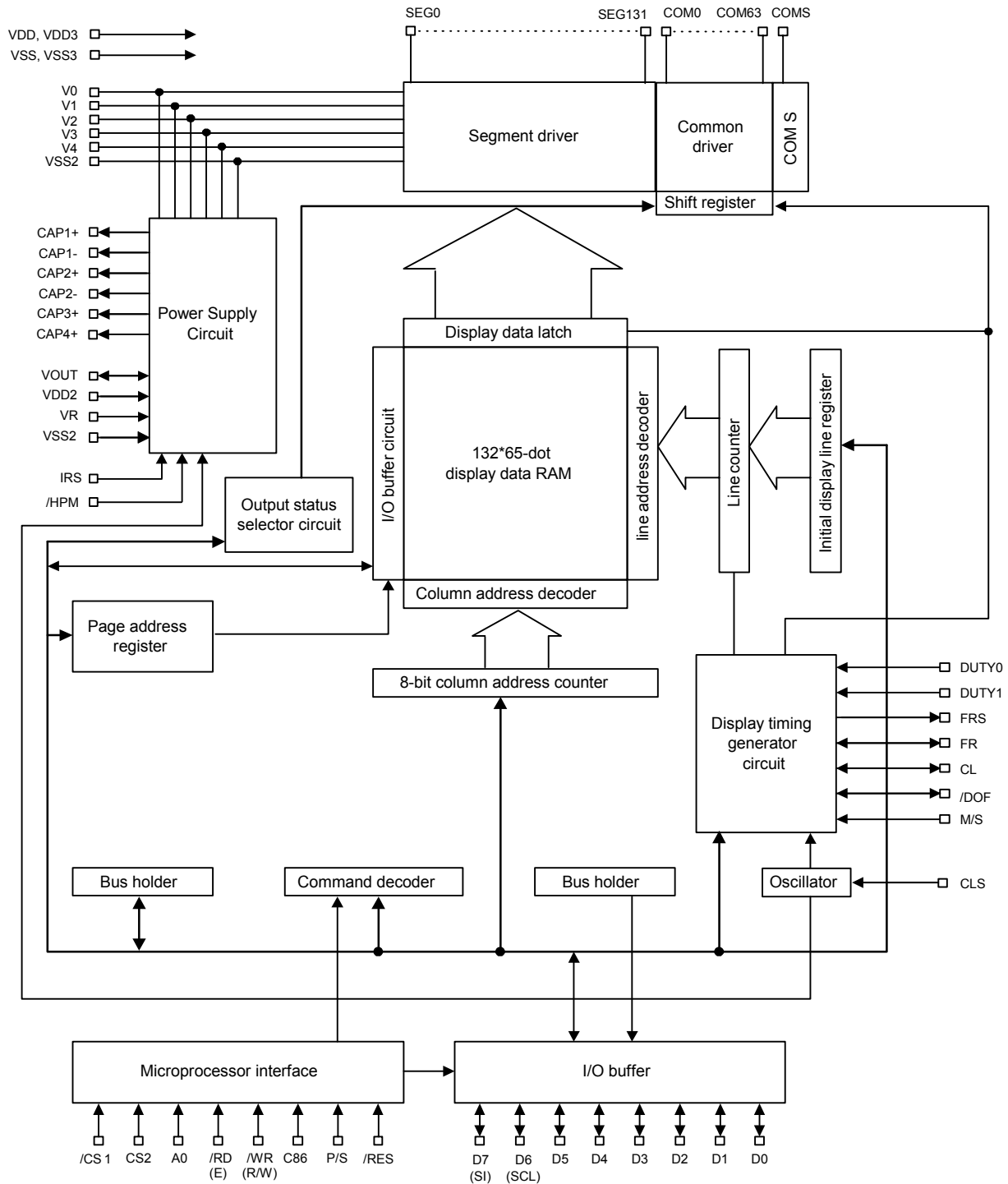
The NT7534 is a single-chip LCD driver for dot-matrix liquid crystal displays, which is directly connectable to a microcomputer bus. It accepts 8-bit parallel or serial display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates an LCD drive signal independent of the microprocessor clock.

The set of the on-chip display RAM of 65 x 132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom. The NT7534 contain 65 common output circuits and 132 segment output circuits, so that a single chip of NT7534 can make maximum 65 x 132 or 49 x 132 or 33 x 132 dots display with the pad option (DUTY1, DUTY0).

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with minimum current consumption and the smallest LSI configuration.



## Block Diagram



**Pad Descriptions**
**Power Supply**

Pad No.	Designation	I/O	Description																																			
42 ~ 44	VDD	Supply	Power supply input. These pads must be connected to each other.																																			
45	VDD3																																					
46 ~ 49	VDD2	Supply	These are the power supply pads for the step-up voltage circuit for the LCD. These pads must be connected to each other.																																			
16, 22, 97, 103, 107	VDD	O	Power supply output for pad option																																			
50 ~ 52	VSS	Supply	Ground. These pads must be connected to each other.																																			
53	VSS3																																					
54 ~ 57	VSS2	Supply	Ground. These pads must be connected to each other.																																			
13, 40, 100, 105	VSS	O	Ground output for pad option.																																			
94, 95	V0	I/O	<p>LCD driver supplies voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship:  <math>V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS2</math>                      When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the LCD Bias Set command.</p> <table border="1"> <thead> <tr> <th>LCD bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/4 bias</td> <td>3/4V0</td> <td>2/4V0</td> <td>2/4V0</td> <td>1/4V0</td> </tr> <tr> <td>1/5 bias</td> <td>4/5V0</td> <td>3/5V0</td> <td>2/5V0</td> <td>1/5V0</td> </tr> <tr> <td>1/6 bias</td> <td>5/6V0</td> <td>4/6V0</td> <td>2/6V0</td> <td>1/6V0</td> </tr> <tr> <td>1/7 bias</td> <td>6/7V0</td> <td>5/7V0</td> <td>2/7V0</td> <td>1/7V0</td> </tr> <tr> <td>1/8 bias</td> <td>7/8V0</td> <td>6/8V0</td> <td>2/8V0</td> <td>1/8V0</td> </tr> <tr> <td>1/9 bias</td> <td>8/9V0</td> <td>7/9V0</td> <td>2/9V0</td> <td>1/9V0</td> </tr> </tbody> </table>	LCD bias	V1	V2	V3	V4	1/4 bias	3/4V0	2/4V0	2/4V0	1/4V0	1/5 bias	4/5V0	3/5V0	2/5V0	1/5V0	1/6 bias	5/6V0	4/6V0	2/6V0	1/6V0	1/7 bias	6/7V0	5/7V0	2/7V0	1/7V0	1/8 bias	7/8V0	6/8V0	2/8V0	1/8V0	1/9 bias	8/9V0	7/9V0	2/9V0	1/9V0
LCD bias	V1			V2	V3	V4																																
1/4 bias	3/4V0			2/4V0	2/4V0	1/4V0																																
1/5 bias	4/5V0			3/5V0	2/5V0	1/5V0																																
1/6 bias	5/6V0			4/6V0	2/6V0	1/6V0																																
1/7 bias	6/7V0			5/7V0	2/7V0	1/7V0																																
1/8 bias	7/8V0	6/8V0	2/8V0	1/8V0																																		
1/9 bias	8/9V0	7/9V0	2/9V0	1/9V0																																		
86, 87	V1																																					
88, 89	V2																																					
90, 91	V3																																					
92, 93	V4																																					

Note: VDD and VDD3 pads must be connected together.

**LCD Power Supply**

Pad No.	Designation	I/O	Description
70 ~ 73	C1-	O	Capacitor 1- pad for internal DC/DC voltage converter.
74 ~ 77	C1+	O	Capacitor 1+ pad for internal DC/DC voltage converter.
82 ~ 85	C2-	O	Capacitor 2- pad for internal DC/DC voltage converter.
78 ~ 81	C2+	O	Capacitor 2+ pad for internal DC/DC voltage converter.
66 ~ 69	C3+	O	Capacitor 3+ pad for internal DC/DC voltage converter.
62 ~ 65	C4+	O	Capacitor 4+ pad for internal DC/DC voltage converter.
59 ~ 61	VOUT	I/O	DC/DC voltage converter output
96	VR	I	Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.

**Configuration Pad**

Pad No.	Designation	I/O	Description												
39, 41	DUTY0 DUTY1	I	Select the maximum LCD driver duty												
			<table border="1"> <thead> <tr> <th>DUTY1</th> <th>DUTY0</th> <th>LCD driver duty</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1/33</td> </tr> <tr> <td>0</td> <td>1</td> <td>1/49</td> </tr> <tr> <td>1</td> <td>*</td> <td>1/65</td> </tr> </tbody> </table>	DUTY1	DUTY0	LCD driver duty	0	0	1/33	0	1	1/49	1	*	1/65
			DUTY1	DUTY0	LCD driver duty										
			0	0	1/33										
0	1	1/49													
1	*	1/65													

**System Bus Connection**

Pad No.	Designation	I/O	Description
23, 24 25, 26 27, 28 29, 30 31, 32 33, 34 35, 36 37, 38	D0 D1 D2 D3 D4 D5 D6 (SCL) D7 (SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.
18	A0	I	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicate that D0 to D7 are display data A0 = "L": Indicates that D0 to D7 are control data
17	/RES	I	When /RES is set to "L", the settings are initialized. The reset operation is performed by the /RES signal level
14 15	/CS1 CS2	I	This is the chip select signal. When /CS1="L" and CS2="H", then the chip select becomes active, and data/command I/O is enabled.
21	/RD (E)	I	When connected to an 8080 MPU, it is active LOW. This pad is connected to the /RD signal of the 8080MPU, and the NT7534 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU
19	/WR (R/W)	I	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W = "H": Read When R/W = "L": Write
101	C86	I	This is the MPU interface switch terminal C86 = "H": 6800 Series MPU interface C86 = "L": 8080 Series MPU interface

**System Bus Connection (continuous)**

Pad No.	Designation	I/O	Description															
102	P/S	I	<p>This is the parallel data input/serial data input switch terminal  P/S = "H": Parallel data input  P/S = "L": Serial data input  The following applies depending on the P/S status:</p> <table border="1"> <thead> <tr> <th>P/S</th> <th>Data/Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>A0</td> <td>D0 to D7</td> <td>/RD, /WR</td> <td>-</td> </tr> <tr> <td>"L"</td> <td>A0</td> <td>SI (D7)</td> <td>Write only</td> <td>SCL (D6)</td> </tr> </tbody> </table> <p>When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. /RD (E) and /WR (R/W) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.</p>	P/S	Data/Command	Data	Read/Write	Serial Clock	"H"	A0	D0 to D7	/RD, /WR	-	"L"	A0	SI (D7)	Write only	SCL (D6)
P/S	Data/Command	Data	Read/Write	Serial Clock														
"H"	A0	D0 to D7	/RD, /WR	-														
"L"	A0	SI (D7)	Write only	SCL (D6)														
99	CLS	I	<p>Terminal to select whether enable or disable the display clock internal oscillator circuit.  CLS = "H": Internal oscillator circuit for display is enabled  CLS = "L": Internal oscillator circuit for display is disabled (requires external input)  When CLS = "L", input the display clock through the CL pad.</p>															
98	M/S	I	<p>This terminal selects the master/slave operation for the NT7534 chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.</p>															
11	CL	I/O	<p>This is the display clock input terminal. When the NT7534 chips are used in master/slave mode, the various CL terminals must be connected.</p>															
10	FR	I/O	<p>This is the liquid crystal alternating current signal I/O terminal  M/S = "H": Output  M/S = "L": Input  When the NT7534 chip is used in master/slave mode, the various FR terminals must be connected.</p>															
12	/DOF	I/O	<p>This is the liquid crystal display blanking control terminal.  M/S = "H": Output  M/S = "L": Input  When the NT7534 chip is used in master/slave mode, the various /DOF terminals must be connected.</p>															
9	FRS	O	<p>This is the output terminal for the static drive. This terminal is only enabled when the static indicator display is ON in master operation mode, and is used in conjunction with the FR terminal</p>															

**System Bus Connection (continuous)**

Pad No.	Designation	I/O	Description
106	IRS	I	<p>This terminal selects the resistors for the V0 voltage level adjustment.</p> <p>IRS = "H", Use the internal resistors            IRS = "L", Do not use the internal resistors</p> <p>The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal. This pad is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected</p>
104	/HPM	I	<p>This is the power control terminal for the power supply circuit for liquid crystal drive.</p> <p>/HPM = "H", Normal power mode            /HPM = "L", High power mode</p> <p>This pad is enabled only when the master operation mode is selected and it is fixed to either "H" or "L" when the slave operation mode is selected.</p>

**Liquid Crystal Drive Pads**

Pad No.	Designation	I/O	Description
145 ~ 276	SEG0 - 131	O	Segment signal output for LCD display.
133 ~ 143 117 ~ 130 108 ~ 114 277 ~ 288 291 ~ 304 2 ~ 7	COM10 - 0 COM24 - 11 COM31 - 25 COM32 - 43 COM44 - 57 COM58 - 63	O	Common signal output for LCD display. When in master/slave mode, the same signal is output by both master and slave
8, 144	COMS	O	These are the COM output terminals for the indicator. Both terminals output the same signal. Do not connect these terminals if they are not used. When in master/slave mode, the same signal is output by both master and slave.

**Test Pad**

Pad No.	Designation	I/O	Description
20 58	TEST0 TEST1	I	Test pads. No connection.

**No Connected Pad**

Pad No.	Designation	I/O	Description
1, 115, 116, 131, 132, 289, 290, 305	DUMMY	-	Dummy pads, No connection.

## Functional Descriptions

### Microprocessor Interface

#### Interface Type Selection

The NT7534 can transfer data via 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI). When high or low is selected for the parity of P/S pad either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data cannot be read out.

**Table 1**

P/S	Type	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D0 to D5
H	Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D0 to D5
L	Serial Input	/CS1	CS2	A0	-	-	-	SI	SCL	(HZ)

“-” Must always be high or low

#### Parallel Interface

When the NT7534 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pad to go high or low as shown in Table 2.

**Table 2**

C86	Type	/CS1	CS2	A0	/RD	/WR	D0 to D7
H	6800 microprocessor bus	/CS1	CS2	A0	E	R/W	D0 to D7
L	8080 microprocessor bus	/CS1	CS2	A0	/RD	/WR	D0 to D7

#### Data Bus Signals

The NT7534 identifies the data bus signal according to A0, E, R/W (/RD, /WR) signals.

**Table 3**

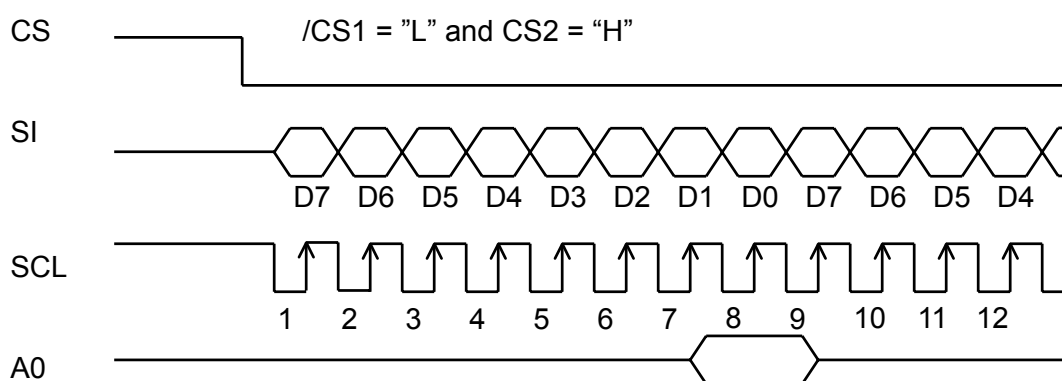
Common	6800 processor	8080 processor		Function
		/RD	/WR	
A0	(R/W)			
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Reads status
0	0	1	0	Writes control data in internal register. (Command)

### Serial Interface

When the serial interface has been selected (P/S = "L"), then when the chip is in active state ( $\overline{CS1}$  = "L" and CS2 = "H"), the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data in the rising edge of eighth serial clock for processing.

The A0 input is used to determine whether or not the serial data input is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection of every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is the serial interface signal chart.

**Figure 1**



Note:

1. When the chip is not active, the shift registers and the counters are reset to their initial states.
2. Reading is not possible while in serial interface mode.
3. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that the operation can be rechecked on the actual equipment.

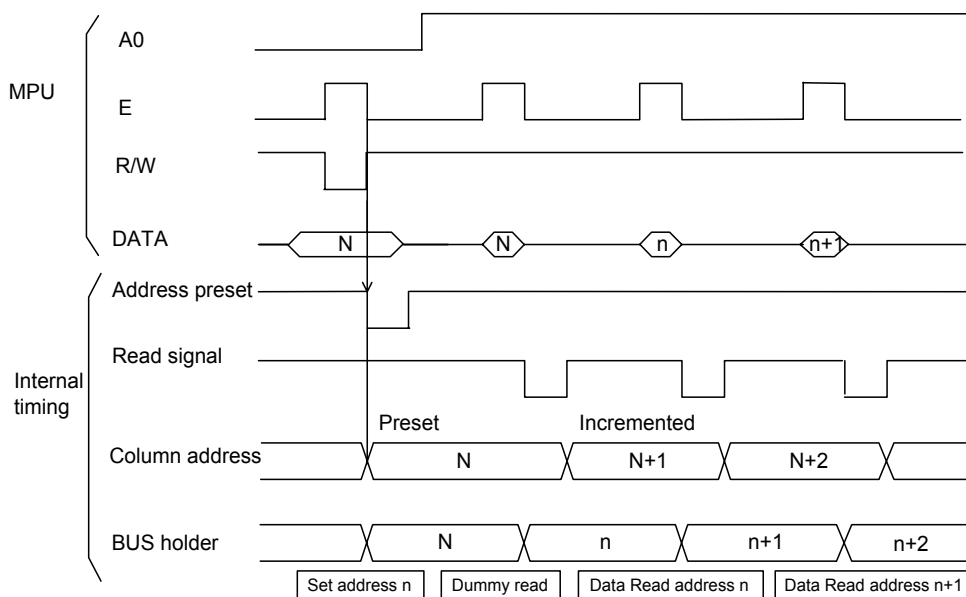
### Chip Select Inputs

The NT7534 has two chip-select pads.  $\overline{CS1}$  and CS2 can interface to a microprocessor when  $\overline{CS1}$  is low and CS2 is high. When these pads are set to any other combination. D0 to D7 are high impedance and A0, E and R/W inputs are disabled. When serial input interface is selected, the shift register and counter are reset.

### Access to Display Data RAM and Internal Registers

The NT7534 can perform a series of pipeline processing between LSI's using the bus holder of the internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in the bus holder, and outputs it onto the system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in the bus holder, and stores it in display RAM until the next data write cycle starts.

When viewed from the microprocessor, the NT7534 access speed greatly depends on the cycle time rather than access time to the display RAM ( $t_{acc}$ ). This view shows that the data transfer speed to / from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during the second data read. A single dummy read must be inserted after address setup and after the write cycle (refer to Figure 2).

**Figure 2**


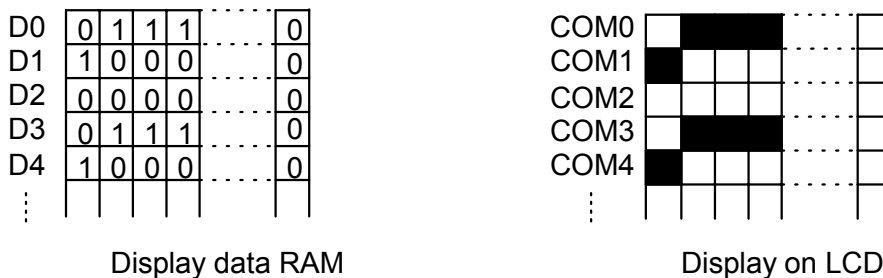
### Busy Flag

When the busy flag is “1” it indicates that the NT7534 chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pad with the read instruction. If the cycle time ( $t_{cyc}$ ) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

### Display Data RAM

The display data RAM is RAM that stores the dot data for the display. It has a 65 (8 page \* 8 bit+1)\*132 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display common direction, and there are few constraints at the time of display data transfer when multiple NT7534 chips are used, thus display structures can be created easily with a high degree of freedom.

Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during the liquid crystal display, it will not cause adverse effects on the display (such as flickering).

**Figure 3**


### The Page Address Circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address8 (D3, D2, D1, D0 = 1, 0, 0, 0,) is the page for the RAM region used; only display data D0 is used.

### The Column Address

As shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read / write command. This allows the MPU display data to be accessed continuously. Moreover, the incrimination of column addresses stops with 83H, because the column address is independent of the page address. Thus, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address.

Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

**Table 4**

SEG Output	SEG0		SEG131
ADC "0"	0 (H)→	Column Address	→83 (H)
(ADC) "1"	83 (H)←	Column Address	←0 (H)

### The Line Address Circuit

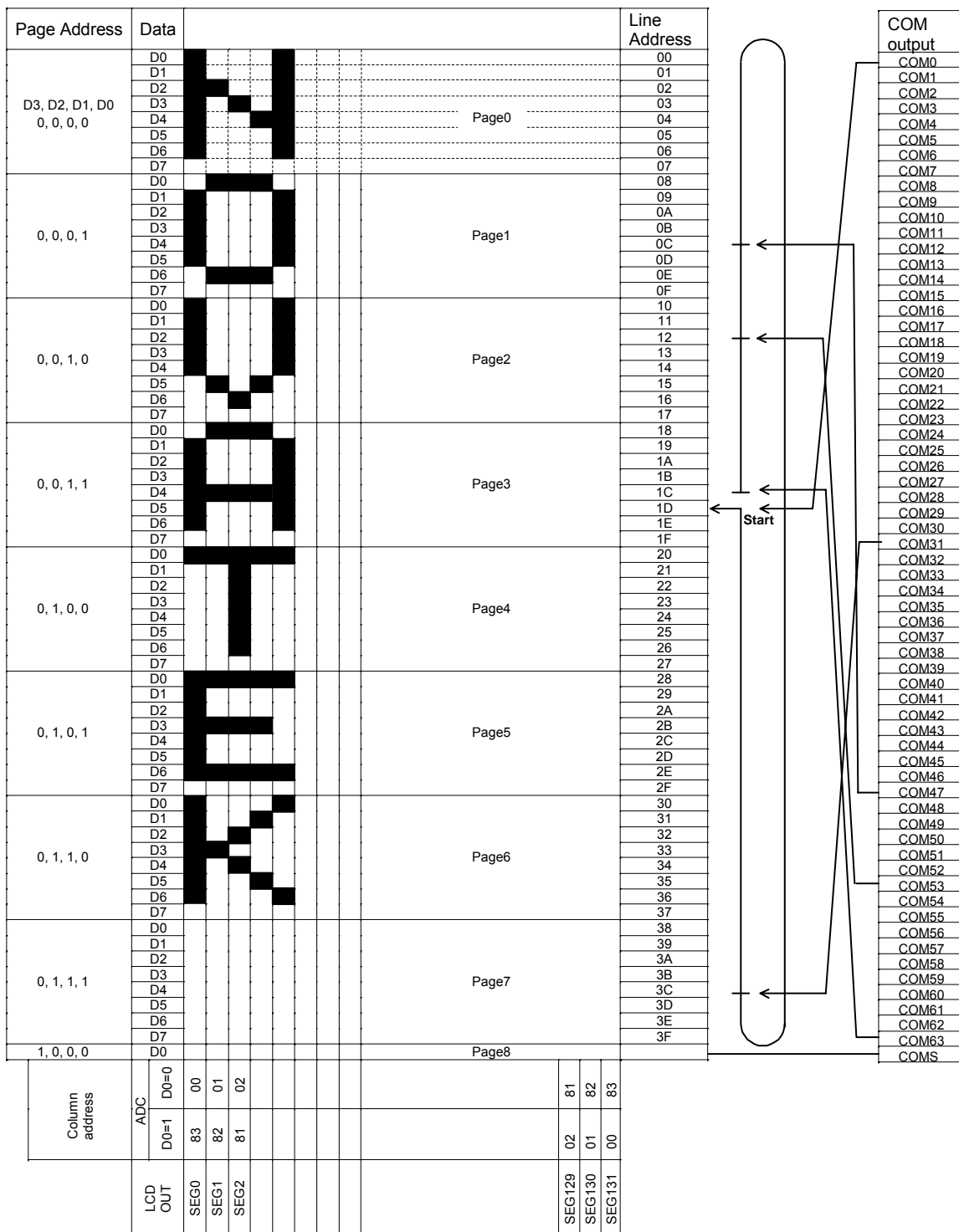
The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal and the COM63 output for NT7534, when the common output mode is reversed. The display area is a 65-line area for the NT7534 from the display start line address. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

### The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

### The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = "H" and CLS = "H". When CLS = "L" the oscillation stops, and the display clock is input through the CL terminal.

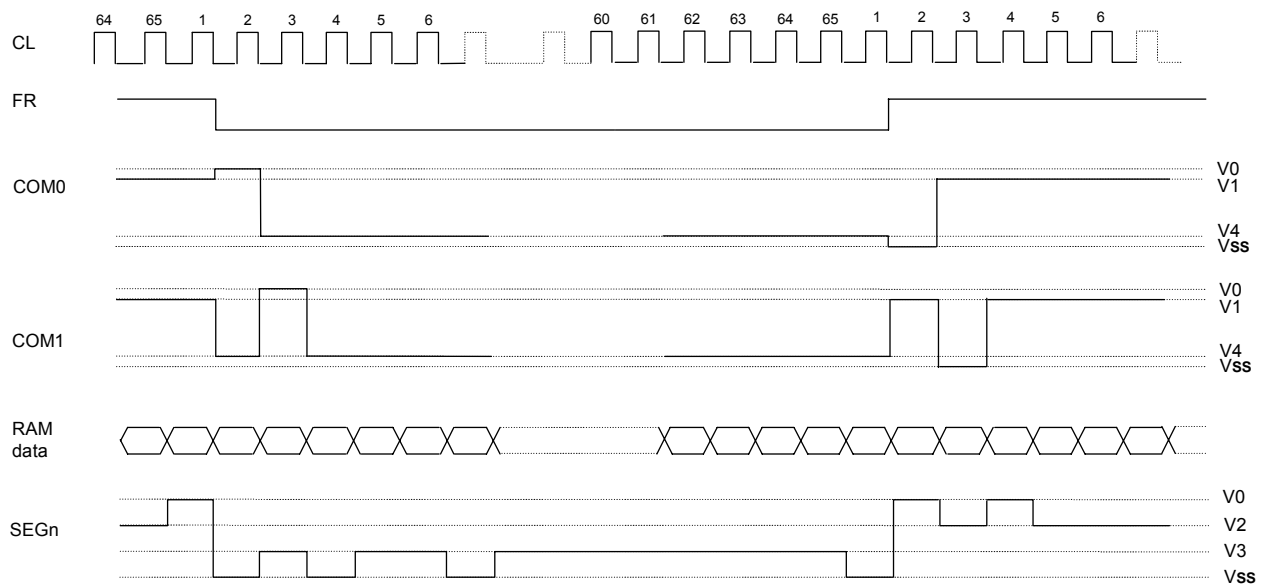
**Figure 4. Relationship between display data RAM and address. (if initial display line is 1DH)**


### Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of access to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive waveform using a 2 frames alternating current drive method, as shown in Figure 5, for the liquid crystal drive circuit.

**Figure 5**



When multiple NT7534 chips are used, the slave chip must be supplied with the display timing signals (FR, CL, /DOF) from the master chip. Table 5 shows the status of the FR, CL, and /DOF signals.

**Table 5**

Operating Mode		FR	CL	/DOF
Master (M/S = "H")	The internal display oscillator is enabled (CLS = "H")	Output	Output	Output
	The internal display oscillator is disabled (CLS = "L")	Output	Input	Output
Slave (M/S = "L")	The internal display oscillator is disabled (CLS = "H")	Input	Input	Input
	The internal display oscillator is disabled (CLS = "L")	Input	Input	Input

Table 6 shows the relationship between oscillation frequency and frame frequency. fOSC can be selected as 31.4K or 26.3KHz by using Oscillation Frequency Select command.

**Table 6**

Duty	Item	fCL	fFR
1/65	On-chip oscillator is used	fOSC/6	fCL/(2 x 65)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 65)
1/49	On-chip oscillator is used	fOSC/8	fCL/(2 x 49)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 49)
1/33	On-chip oscillator is used	fOSC/12	fCL/(2 x 33)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 33)
1/17	On-chip oscillator is used	fOSC/22	fCL/(2 x 17)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 17)
1/9	On-chip oscillator is used	fOSC/44	fCL/(2 x 9)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 9)

### Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads.

**Table 7**

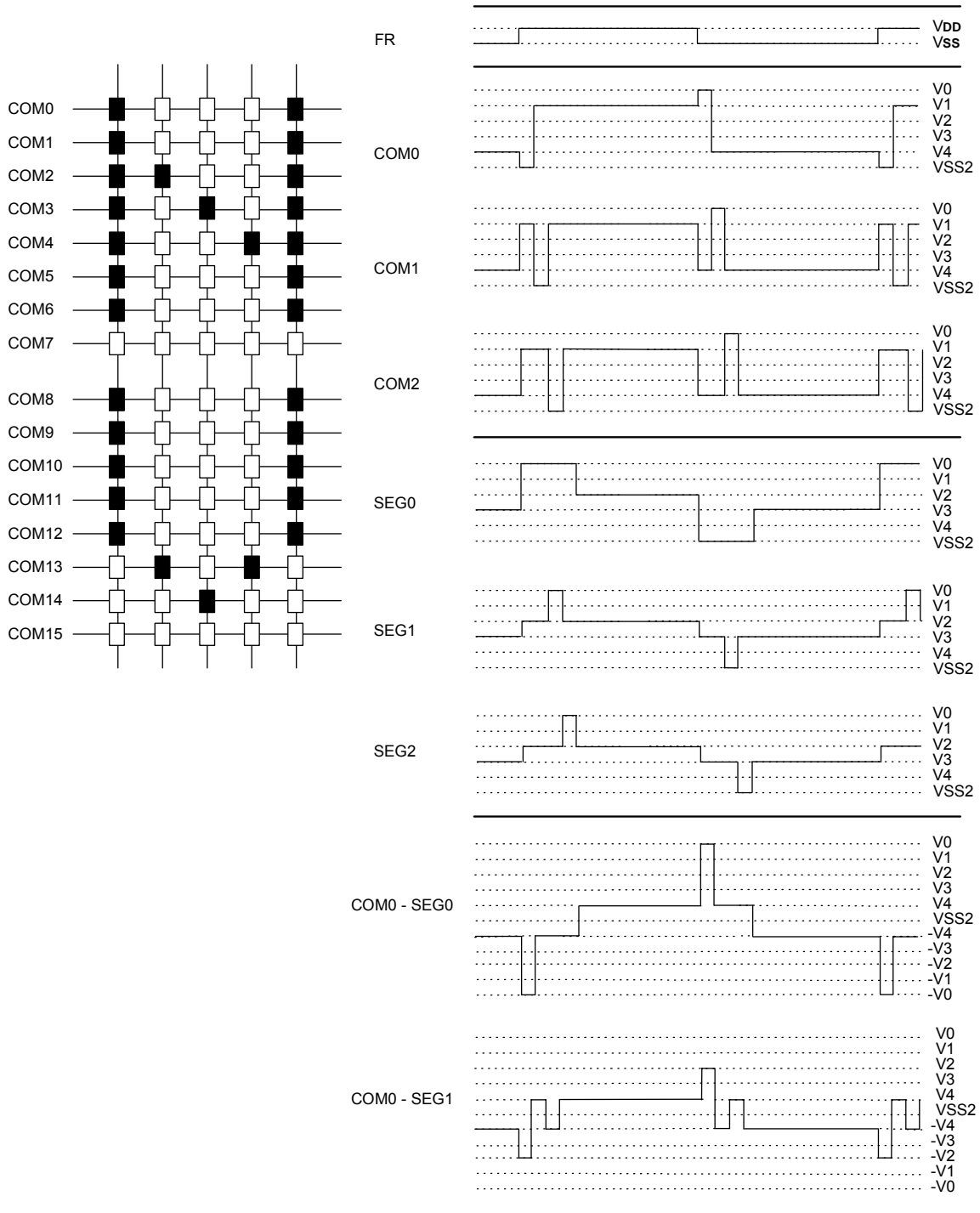
Duty	Status	Common output pads								
		COM [0-15]	COM [16-23]	COM [24-26]	COM [27-36]	COM [37-39]	COM [40-47]	COM [48-63]	COMS	
1/33	Normal	COM[0-15]	NC					COM[16-31]	COMS	
	Reverse	COM[31-16]	NC					COM[15-0]		
1/49	Normal	COM[0-23]		NC			COM[24-47]		COMS	
	Reverse	COM[47-24]		NC			COM[23-0]			
1/65	Normal	COM[0-63]								COMS
	Reverse	COM[63-0]								

The combination of the display data, the COM scanning signals, and the FR signal produces the liquid crystal drive voltage output. Figure 6 shows example of the SEG and COM output waveform.

### Configuration Setting

The NT7534 has two optional configurations, configured by DUTY0, DUTY1.

DUTY1, DUTY0	Common	Segment	V1	V2	V3	V4
1, 0 or 1, 1	65	132	8/9V0, 6/7V0	7/9V0, 5/7V0	2/9V0, 2/7 V0	1/9V0, 1/7V0
0, 1	49	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 0	33	132	5/6V0, 4/5V0	4/6V0, 3/5V0	2/6 V0, 2/5V0	1/6V0, 1/5V0

**Figure 6**


### The Power Supply Circuit

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 8 shows the Power Control Set Command 3-bit data control functions, and Table 9 shows reference combinations.

**Table 8**

Item	Status	
	"1"	"0"
D2 Voltage Booster (V/B) circuit control bit	ON	OFF
D1 Voltage regulator (V/R) circuit control bit	ON	OFF
D0 Voltage follower (V/F) circuit control bit	ON	OFF

**Table 9**

Use Settings	D2	D1	D0	V/B Circuit	V/R circuit	V/F circuit	External voltage input	Step-up voltage system terminal
Only the internal power supply is used	1	1	1	ON	ON	ON	VDD2	Used
Only the V/R circuit and the V/F circuit are used	0	1	1	OFF	ON	ON	VOUT, VDD2	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V0, VDD2	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V0 to V4	Open

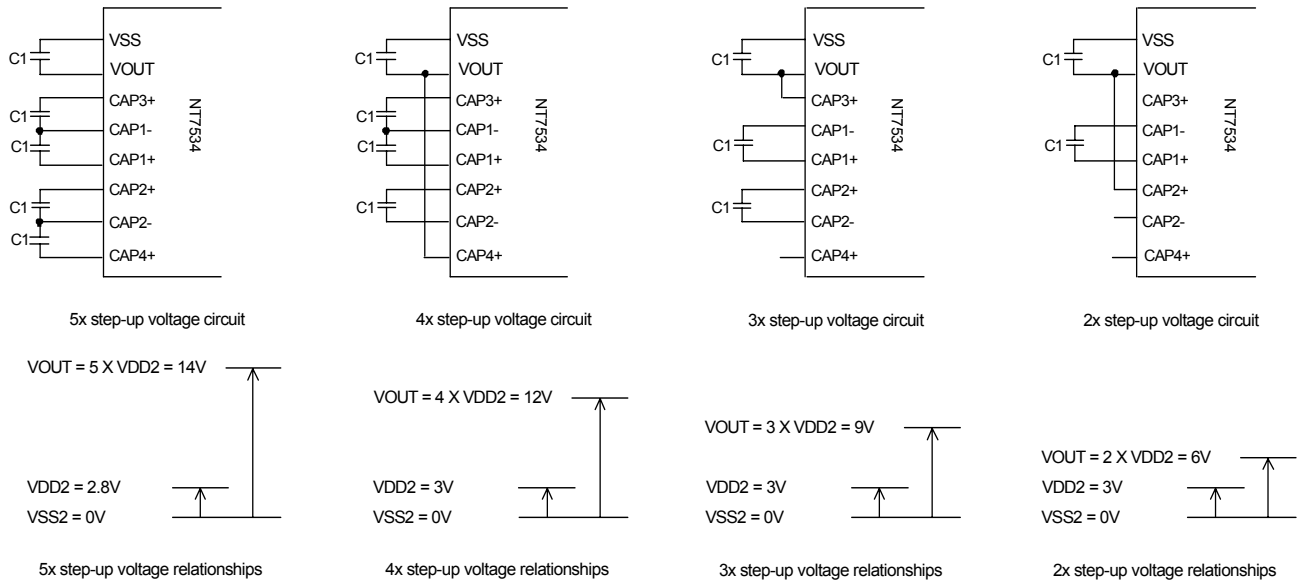
\*The "Step-up system terminals" refer CAP1+, CAP1-, CAP2+, CAP2-, CAP3+ and CAP4+.

\*While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

## The Step-up Voltage Circuits

Using the step-up voltage circuits within the NT7534 chips it is possible to product 5X, 4X, 3X, 2X step-ups of the VDD2-VSS2 voltage levels.

**Figure 7**



## The Voltage Regulator Circuit

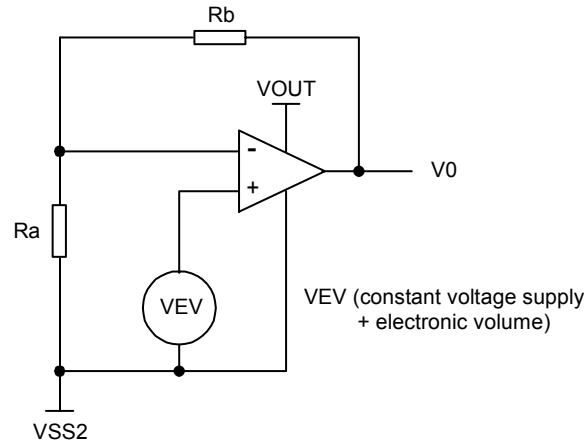
The step-up voltage generated at VOUT outputs the liquid crystal driver voltage V0 through the voltage regulator circuit. Because the NT7534 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

Moreover, **NT7534 has thermal gradients: approximately  $-0.05\%/^{\circ}C$ .**

### When the V0 Voltage Regulator Internal Resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where V0 < VOUT.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times VEV = \left(1 + \frac{Rb}{Ra}\right) \times \left(1 - \frac{63 - \alpha}{162}\right) \times VREG \quad (\text{Equation A-1})$$



VREG is the IC internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 10.

**Table 10**

Equipment Type	Thermal Gradient	Units	VREG
Internal Power Supply	-0.05	%/°C	2.1

$\alpha$  is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 11 shows the value for  $\alpha$  depending on the electronic volume register settings. Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1+Rb/Ra) ratio assumes the values shown in Table 12 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

**Table 11**

D5	D4	D3	D2	D1	D0	$\alpha$	V0
0	0	0	0	0	0	0	Minimum
0	0	0	0	0	1	1	:
0	0	0	0	1	0	2	:
		:			:	:	:
1	0	0	0	0	0	32	(default)
		:			:	:	:
1	1	1	1	1	0	62	:
1	1	1	1	1	1	63	Maximum

V0 voltage regulator internal resistance ratio register value and  $(1 + R_b/R_a)$  ratio (Reference value)

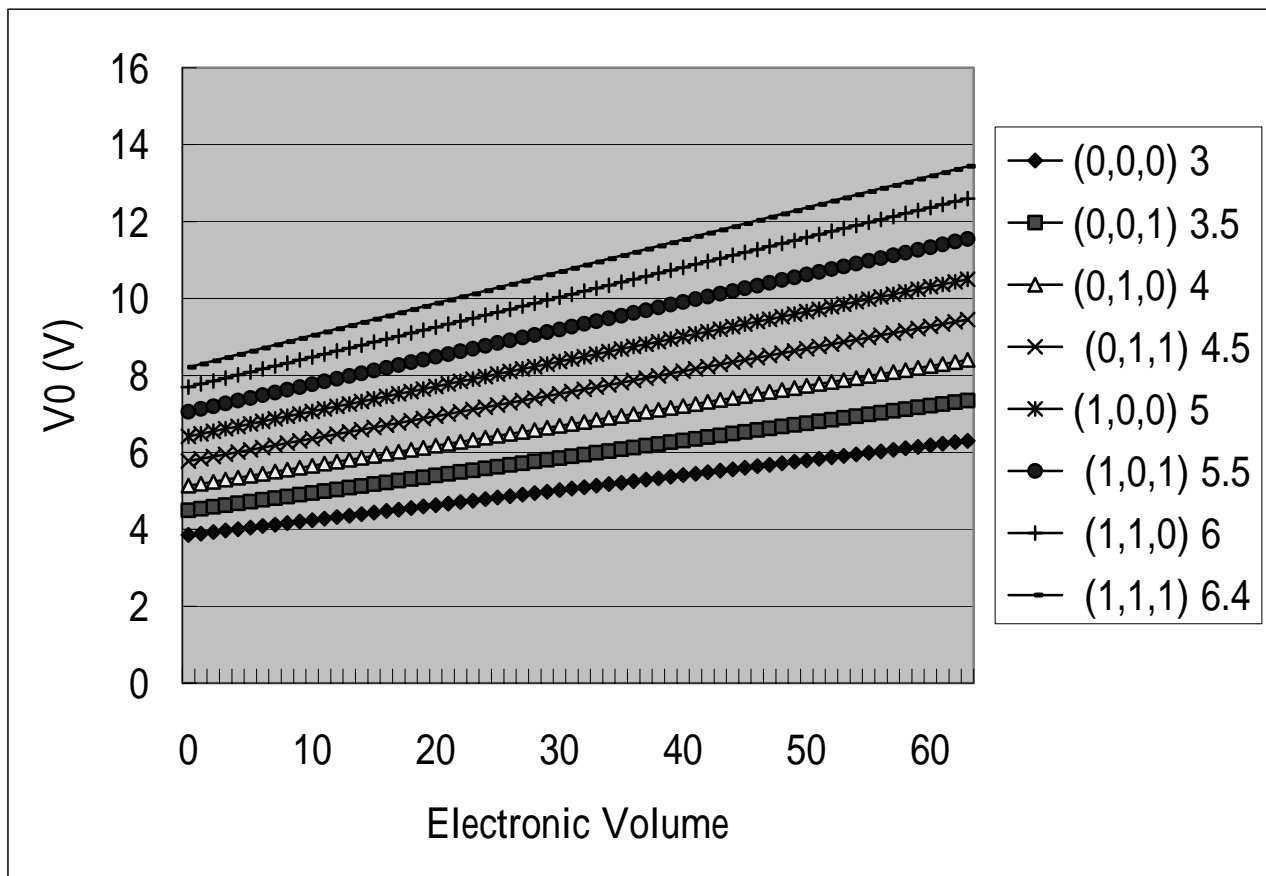
**Table 12**

Register			Equipment Type by Thermal Gradient [Units:%/°C]
D2	D1	D0	-0.05
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0 (default)
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

Note: When selecting external  $R_b/R_a$  resistors,  $R_a + R_b$  should be greater than  $1.5M\Omega$ .

**Figure 8. The Contrast Curve of V0 Voltage with internal resistors**



Setup example: When selecting  $T_a=25^{\circ}\text{C}$  and  $V_0=7\text{V}$  for a NT7534 model on which the temperature compensation is internal, using the equation A-1, the following setup is enable.

**Table 13**

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V0 voltage regulator	-	-	-	0	1	0
Electronic Volume	1	0	0	1	0	1

- When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
- The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L"). When the V0 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the VR terminal is left open.
- Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

#### **The Liquid Crystal Voltage Generator Circuit**

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3, and V4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for NT7534 can be selected when the duty is 1/65.

### High Power Mode

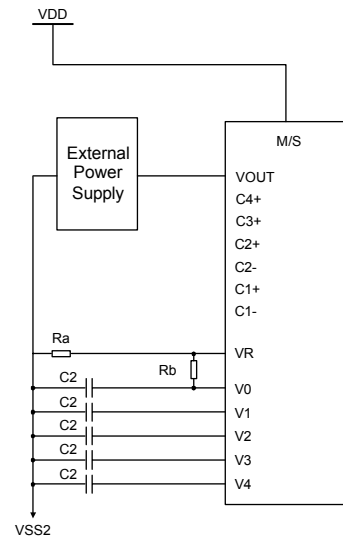
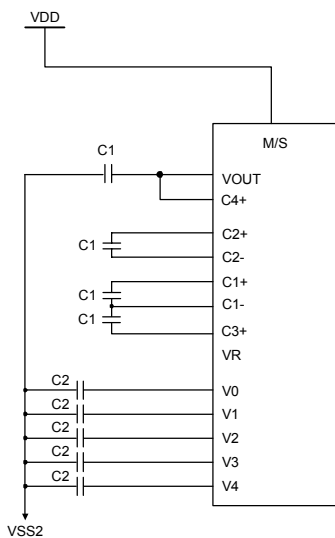
The power supply circuit equipped in the NT7534 chips has very low power consumption (normal mode: /HPM="H"). However for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the /HPM terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.

Moreover, if the improvement to the display is inadequate even after the high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

### Reference Power Supply Circuit for Driving LCD Panel

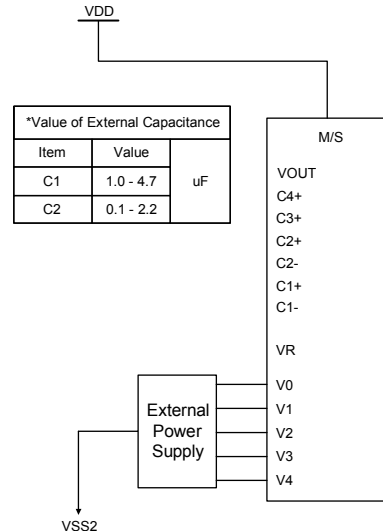
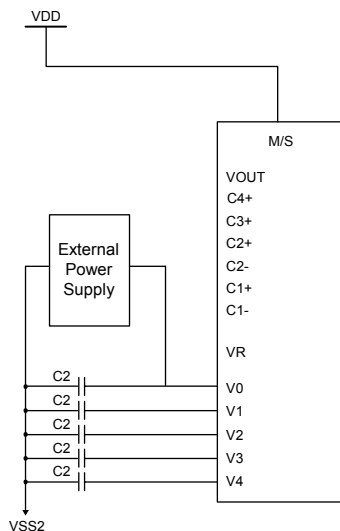
-When using all LCD power circuits  
(Voltage booster, regulator and follower)  
(In case of 4X boosting circuit and internal regulator resistors, IRS=1)

--When not using voltage booster circuits  
(In case of external regulator resistors, IRS=0)



-When only using voltage follower

-When not using internal LCD power supply circuits



## Reset Circuit

When the /RES input falls to “L”, these LSIs reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = “L”)
4. Power control register (D2, D1, D0) = (0, 0, 0,)
5. Register data clear in serial interface
6. LCD power supply bias ratio 1/9 (1/65 duty), 1/8 (1/49 duty), 1/6 (1/33 duty)
7. Read modify write OFF
8. Static indicator: OFF  
Static indicator register: (D1, D2) = (0, 0)
9. Display start line register set at first line
10. Column address counter set at address 0
11. Page address register set at page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear:  
V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear  
Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Test mode clear
16. Oscillation frequency 31.4 KHz
17. Normal display mode and frame inversion status (partial display and N-Line inversion release)
18. Partial display duty register: (D2, D1, D0) = (1, 0, 0), 1/65 duty
19. Partial display bias register: (D2, D1, D0) = (1, 0, 1), 1/9 bias
20. N-Line inversion register: (D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0), 13-Line inversion
21. Partial start line register: (D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0), the first line
22. DC/DC clock division register: (D3, D2, D1, D0) = (0, 0, 1, 1), fOSC/6
23. Output condition of COM, SEG  
COM: VSS  
SEG: VSS

On the other hand, when the reset command is used, only default settings 7 to 15 above are put into effect.

The MPU interface (Reference Example), the /RES terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RES terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition; therefore, take measures to prevent the input terminal from entering a high impedance state.

In the NT7534, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply an “L” signal to the /RES terminal when the external liquid crystal power supply is applied. Even though the oscillator circuit operates while the /RES terminal is “L,” the display timing generator circuit is stopped, and the FR, FRS, and /DOF terminals are fixed to “H,” and the CL pin is fixed to “H” only when the internal oscillator circuit is used. There is no influence on the D0 to D7 terminals.

## Commands

The NT7534 uses a combination of A0, /RD (E) and /WR (R/W) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the /RD pad and a write status when a low pulse is input to the /WR pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/W pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, /RD (E) becomes 1(high) when the 6800 series microprocessor interface reads status of display data. This is the only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands are explained below. When the serial interface is selected, input data starting from D7 in sequence.

### 1. Display ON/OFF

Alternatively turns the display on and off.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	1	1	AFh	Display ON
										0	AEh	Display OFF

When the display OFF command is executed when in the display all points ON mode, power save mode is entered. See the section on the power saver for details.

### 2. Display Start Line Set

Specifies line address (refer to Figure 6) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. The higher number of lines in ascending order, corresponding to the duty cycle follows it. When this command changes the line address, smooth scrolling or a page change takes place.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	A5	A4	A3	A2	A1	A0	40h to 7Fh

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

### 3. Page Address Set

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator, and only D0 is valid for data change.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	1	1	A3	A2	A1	A0	B0h to B8h

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
		:		:
0	1	1	1	7
1	0	0	0	8

### 4. Column Address Set

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access the display RAM, the column address counter is incremental by during each access until address 132 is accessed. The page address is not changed during this time.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
0	1	0	0	0	0	1	A7	A6	A5	A4	10h to 18h	High nibble
						0	A3	A2	A1	A0	00h to 0Fh	Low nibble

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	1
0	0	0	1	0	1	1	0	2
			:					:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

**5. Read Status**

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	/ADC	OFF/ON	RESET	0	0	0	0

**BUSY:** When high, the NT7534 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

**/ADC:** Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address “131-n” corresponds to segment driver n. when high, the display is normal and column address corresponds to segment driver n.

**OFF/ON:** Indicates whether the display is on or off. When low, the display turns on. When high, the display turns off. This is the opposite of Display ON/OFF command.

**RESET:** Indicates the initialization is in progress by /RES signal or by reset command. When low, the display is on. When high, the chip is being reset.

**6. Write Display Data**

Write 8-bit data in display RAM. As the column address automatically increments by 1 after each write, the microprocessor can continue to write data of multiple words.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

**7. Read Display Data**

Reads 8-bit data from display RAM area specified by column address and page address. As the column address automatically increments by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

**8. ADC Select**

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads could be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	0	0	0	A0h	Normal
										1	A1h	Reverse

**9. Normal/ Reverse Display**

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	1	0	A6h	RAM Data "H" LCD ON voltage (normal)
										1	A7h	RAM Data "L" LCD ON voltage (reverse)

**10. Entire Display ON**

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	0	0	A4h	Normal display mode
										1	A5h	Display all points ON

When D0 is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power save mode. Refer to the Power Save section for details.

**11. LCD Bias Set**

This command selects the voltage bias ratio required for the liquid crystal display.

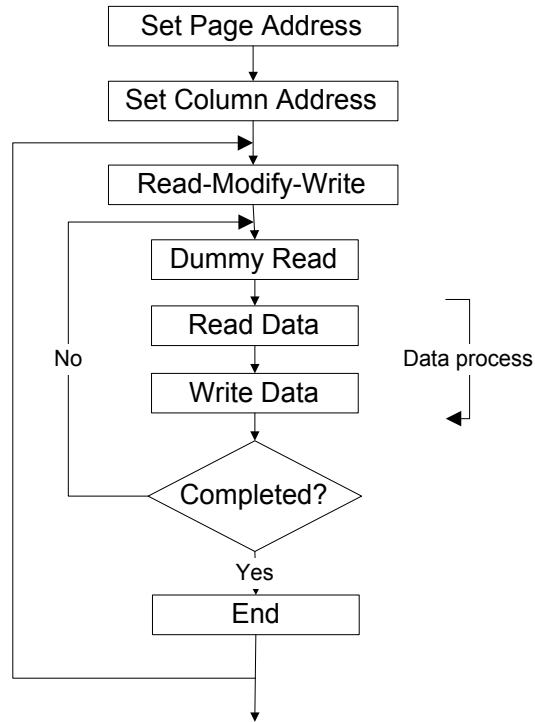
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Duty		
												1/33	1/49	1/65
0	1	0	1	0	1	0	0	0	1	0	A2h	1/6 bias	1/8 bias	1/9 bias
										1	A3h	1/5 bias	1/6 bias	1/7 bias

**12. Read-Modify-Write**

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or other events.

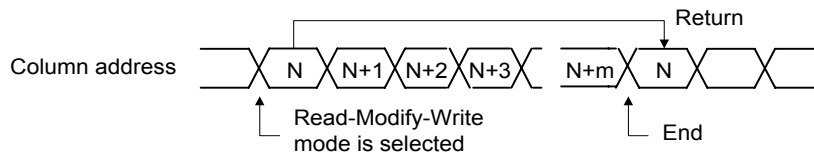
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	0	0	E0h

Note: Any command except Read/Write Display Data and Column Address Set can be issued during Read-Modify-Write mode.

**Cursor display sequence**

**13. End**

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued)

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	1	1	1	0	Eh



**14. Reset**

This command resets the Display Start Line register, Column Address counter, Page Address register, and Common output mode register, the V0 voltage regulator internal resistor ratio register, the Electronic Volume register, the static indicator mode register, the read-modify-write mode register, and the test mode. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
/RD	/WR										
0	1	0	1	1	1	0	0	0	1	0	E2h

The Reset command cannot initialize LCD power supply. Only the Reset signal to the /RES pad can initialize the supplies.

**15. Output Status Select Register**

When D3 is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
/RD	/WR										
0	1	0	1	1	0	0	0	*	*	*	C0h to C7h
							1				C8h to CFh

\*: Invalid bit

D3 = 0: Normal (COM0 → COM63/47/31)

D3 = 1: Reverse (COM63/47/31 → COM0)

**16. Power Control Set**

Select one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
/RD	/WR										
0	1	0	0	0	1	0	1	A2	A1	A0	28h to 2Fh

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.

When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.

When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

**17. V0 Voltage Regulator Internal Resistor Ratio Set**

This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under “The Power Supply Circuits”.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	20h	Small
								0	0	1	21h	
								0	1	0	22h	
									:		:	:
								1	1	0	26h	
								1	1	1	27h	Large

**18. The Electronic Volume (Double Byte Command)**

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. It is a two-byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

**(1) The Electronic Volume Mode Set**

When this command is input, the electronic volume register set command is enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	0	0	1	81h

**(2) Electronic Volume Register Set**

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	V0
0	1	0	*	*	0	0	0	0	0	1	XX	Small
					0	0	0	0	1	0	XX	
									:		:	:
					1	1	1	1	1	0	XX	
					1	1	1	1	1	1	XX	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

**19. Static Indicator (Double Byte Command)**

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double bytes command paired with the static indicator register set command, and thus command must be executed one after the other. (The static indicator OFF command is a single byte command)

**(1) Static Indicator ON/OFF**

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	0	0	ACh	Static Indicator OFF
										1	ADh	Static Indicator ON

**(2) Static Indicator Register Set**

This command sets two bits of data into the static indicator register and used to set the static indicator into a blinking mode.

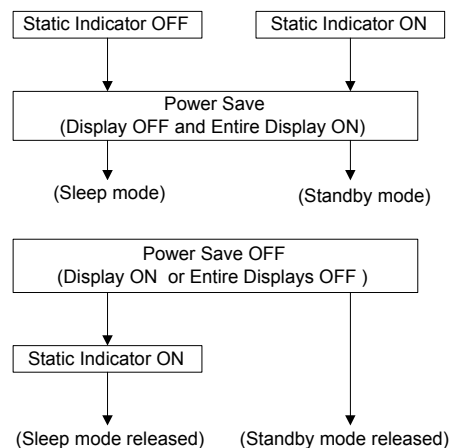
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Indicator Display Status
0	1	0	*	*	*	*	*	*	0	0	XX	OFF
									0	1	XX	ON (blinking at approximately 1 second intervals)
									1	0	XX	ON (blinking at approximately 0.5 second intervals)
									1	1	XX	ON (constantly on)

## 20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce current consumption.

If the static indicator is off, the Power Save command makes the system enter sleep mode. If the static indicator is on, this command makes the system enter standby mode.

Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



### Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

- (1) Stops the oscillator circuit and LCD power supply circuit.
- (2) Stops the LCD driver and outputs the VSS level as the segment/common driver output.
- (3) Holds the display data and operation mode provided before the start of the sleep mode.
- (4) The MPU can access the built-in display data RAM.

### Standby Mode

Stops the operation of the duty LCD displays system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive. The ON operation of the static drive system indicates that the NT7534 is in standby mode. The internal status in the standby mode is as follows:

- (1) Stops the LCD power supply circuit.
- (2) Stops the LCD drive and outputs the VSS level as the segment / common driver output.  
However, the static drive system still operates.
- (3) Holds the display data and operation mode provided before the start of the standby mode.
- (4) The MPU can access the built-in display data RAM.

When the Reset command is issued in the standby mode, the sleep mode is set.

- When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7534 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7534 to go to the sleep mode or standby mode.

**21. NOP**

Non-Operation Command.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
/RD	/WR										
0	1	0	1	1	1	0	0	0	1	1	E3h

**22. Test Command**

This is the dedicated IC chip test command. It must not be used for normal operation. If the Test command is issued inadvertently, set the /RES input to low or issue the Reset command to release the test mode.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
/RD	/WR										
0	1	0	1	1	1	1	0	1	0	0	F0h to FFh

\*: Invalid bit

**Cautions:** The NT7534 maintains an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. Users must consider how to suppress noise on the package and system or to prevent ambient noise insertion. To prevent a spike in noise, built-in software for periodical status refreshment is recommended. The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

**23. Oscillation Frequency Select**

This command is to select the oscillation frequency of driver IC as below.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Oscillation Frequency
/RD	/WR											
0	1	0	1	1	1	0	0	1	0	0	E4h	Typical 31.4 KHz
										1	E5h	Typical 26.3 KHz

**24. Partial Display Mode Set**

This command enables to select the display mode. When D0 is low, the IC is in normal display mode, the maximum display duty ratio is decided by pin connection of DUTY0 and DUTY1 and the command LCD Bias Set decides the LCD bias ratio. The IC enters into partial display mode when D0 is high, then the commands Partial Display Duty Set and Partial Display Bias Set decide the LCD display duty and bias ratios.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Display Mode
0	1	0	1	0	0	0	0	0	1	0	82h	Normal Display
										1	83h	Partial Display

**25. Partial Display Duty and Bias Set**

These two commands set the LCD display duty and bias ratios when the IC is in partial display mode. They are invalid when the IC is in normal display mode. When the partial display duty is set, the LCD bias for partial display is set simultaneous as below. The partial display duty will be kept at maximum duty (decided by pins DUTY0 and DUTY1) when setting duty is larger than maximum duty.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Duty	Scanning Line
0	1	0	0	0	1	1	0	0	0	0	30h	1/9 duty	Line [0:7], COMS
								0	0	1	31h	1/17 duty	Line [0:15], COMS
								0	1	0	32h	1/33 duty	Line [0:31], COMS
								0	1	1	33h	1/49 duty	Line [0:47], COMS
								1	0	0	34h	1/65 duty	Line [0:63], COMS
								1	0	1	35h	Reserved	No effect
								1	1	*	37h	Reserved	No effect

Using Partial Display Bias Set command to change the LCD bias in partial display mode.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	LCD Bias
0	1	0	0	0	1	1	1	0	0	0	38h	1/4
								0	0	1	39h	1/5
								0	1	0	3Ah	1/6
								0	1	1	3Bh	1/7
								1	0	0	3Ch	1/8
								1	0	1	3Dh	1/9
								1	1	0	3Eh	Reserved
								1	1	1	3Fh	Reserved

Note: The COM waveform of no display area is non-select waveform.

**26. Partial Start Line Set (Double Byte Command)**

This command makes it possible to set the partial start line for partial display. It is a two-byte command used as a pair and the Number of Start Line Set command must be issued after the Partial Start Line Set command.

**(1) Partial Start Line Set**

When this command is input, no other command except for the Number of Start Line Set command can be used.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	0	1	0	0	1	1	D3h

**(2) Number of Start Line Set**

By using this command to set six bits of data to the Partial Start Line register. Once the Number of the Start Line Set command has been used to set data into the register, then the partial start line will affect on the LCD display. The number of partial start line is always equal to zero when the partial start line is larger than maximum duty ratio (decided by pins DUTY0 and DUTY1).

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Start Line
0	1	0	*	*	0	0	0	0	0	0	XX	0 line
					0	0	0	0	0	1	XX	1 line
					0	0	0	0	1	0	XX	2 line
								:			:	:
					1	1	1	1	1	0	XX	62 line
					1	1	1	1	1	1	XX	63 line

**27. The N-Line Inversion (Double Byte Command)**

This command makes it possible to adjust the number of scan lines for liquid crystal display inversion. It is a two-byte command used as a pair and the Number of Line Set command must be issued after the N-Line Inversion Set command.

**(1) N-Line Inversion Set**

When this command is input, no other command except for the Number of Line Set command can be used.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	1	0	1	85h

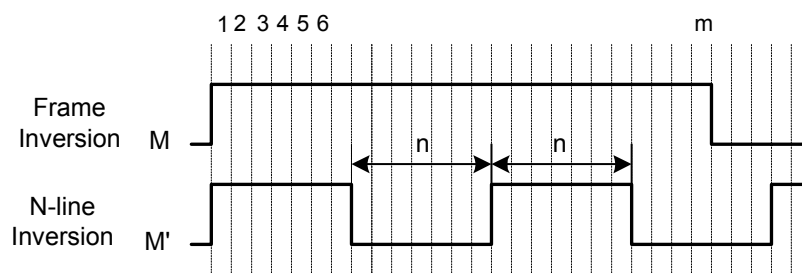
**(2) Number of Line Set**

By using this command to set five bits of data to the N-Line inversion register. Once the Number of Line Set command has been used to set the data into the register, then the N-Line inversion will affect on the LCD display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Line Inversion
0	1	0	*	*	*	0	0	0	0	0	XX	1 line
						0	0	0	0	1	XX	2 line
								:			:	:
						1	1	1	1	1	XX	32 line

Note 1: The number of inversed scan line = register setting value + 1.

Note 2: When Partial Duty = 1/9 or 1/17, the N-line inversion function release and the LCD display scan line is back to frame inversion status.


**28. Release N-Line Inversion**

This command is used to exit the N-Line inversion function. The N-Line inversion function is released and the LCD display is set back to frame inversion status once this command is executed.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	1	0	0	84h

**29. DC/DC Clock Frequency (Double Byte Command)**

This command makes it possible to adjust the frequency for DC/DC clock. It is a two-byte command used as a pair and the DC/DC Frequency Division Set command must be issued after the DC/DC Clock Set command.

**(1) DC/DC Clock Set**

When this command is input, no other command except for the DC/DC Frequency Division Set command can be used.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	1	1	0	E6h

**(2) DC/DC Frequency Division Set**

By using this command to set five bits of data to the frequency division register.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Division
0	1	0	*	*	*	*	0	0	0	0	XX	fOSC
							0	0	0	1	XX	fOSC/2
							0	0	1	0	XX	fOSC/4
							0	0	1	1	XX	fOSC/6 (default)
							0	1	0	0	XX	fOSC/8
							0	1	0	1	XX	fOSC/10
							0	1	1	0	XX	fOSC/12
							0	1	1	1	XX	fOSC/14
							1	0	0	0	XX	fOSC/16
							1	0	0	1	XX	fOSC/18
							1	0	1	0	XX	fOSC/20
							1	0	1	1	XX	fOSC/22
							1	1	0	0	XX	fOSC/24
							1	1	0	1	XX	fOSC/26
1	1	1	0	XX	fOSC/28							
1	1	1	1	XX	fOSC/30							

**Table 14. Command Table**

Command	A0	/RD	/WR	Code								Hex	Function	
				D7	D6	D5	D4	D3	D2	D1	D0			
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0	1	A Eh A Fh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address					40h to 7Fh	Specifies RAM display line for COM0		
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Set the display data RAM page in Page Address register	
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address			00h to 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register		
	0	1	0	0	0	0	0	Lower Column Address						
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information	
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM	
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM	
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0	1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0	1	A6h A7h	Normal indication when low, but full indication when high
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	A4h A5h	Select normal display (0) or entire display on
(11) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0	1	A2h A3h	Sets LCD driving voltage bias ratio
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	0	E0h	Increments column address counter during each write
(13) End	0	1	0	1	1	1	0	1	1	1	0	0	E E h	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	0	E2h	Resets internal functions
(15) Common Output Mode Select	0	1	0	1	1	0	0	0	1	*	*	*	C0h to C F h	Select COM output scan direction *: invalid data
(16) Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode	
(17) V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode	
(18) Electronic Volume mode Set Electronic Volume Register Set	0	1	0	1	0	0	0	0	0	0	1	0	81h	
	0	1	0	*	*	Electronic Control Value					XX	Sets the V0 output voltage electronic volume register		
(19) Set Static indicator ON/OFF Set Static Indicator Register	0	1	0	1	0	1	0	1	1	0	0	1	A Ch A D h	Sets static indicator ON/OFF 0: OFF, 1: ON
	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode	
(20) Power Save	0	1	0	-	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	0	E3h	Command for non-operation

**Command Table (continue)**

Command	A0	/RD	/WR	Code									Hex	Function
				D7	D6	D5	D4	D3	D2	D1	D0			
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0	1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0	1	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode	
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode	
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set	
Partial Start Line Set	0	1	0	1	1	Partial Start Line					XX	Sets the LCD Number of partial display start line		
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion	
Number of Line Set	0	1	0	*	*	*	Number of Line				XX	Sets the number of line used for N-Line inversion		
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion	
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency	
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division			XX	Set the Division of DC/DC Clock Frequency		
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!	
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset	

Note: Do not use any other command, or system malfunction may result.

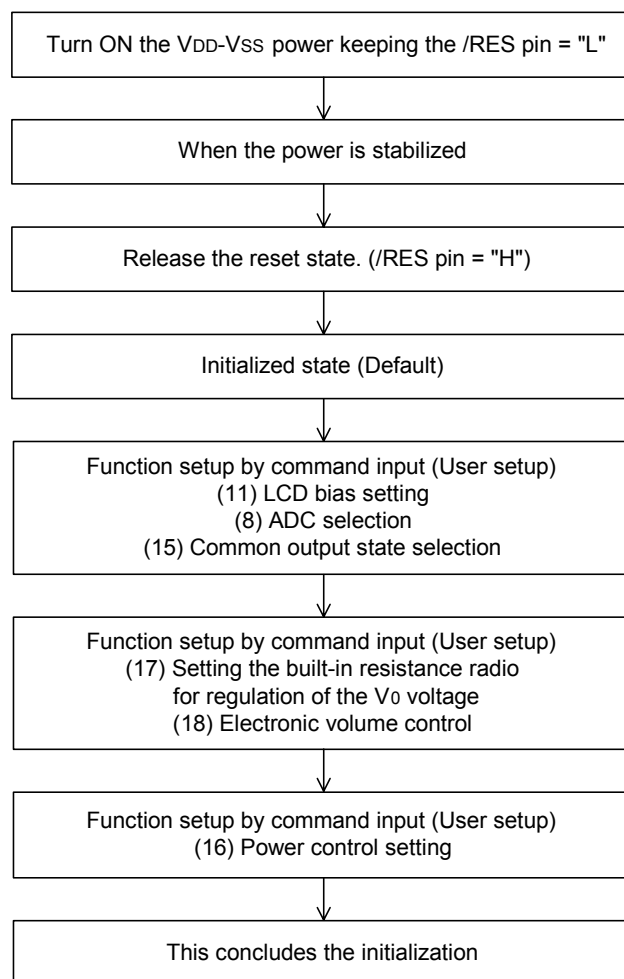
## Command Description

### Instruction Setup: Reference

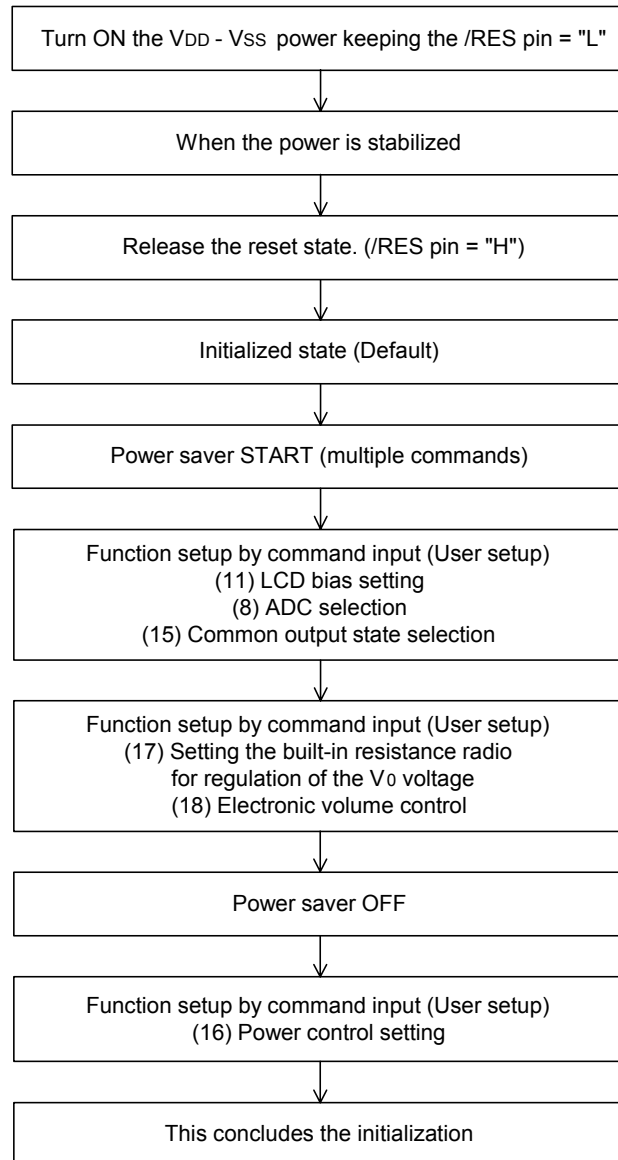
#### 1. Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 - V4) and the VDD pin, the picture on the display may instantaneously become totally dark when the power is turned on. To avoid such failure, we recommend the following flow sequence when turning on the power.

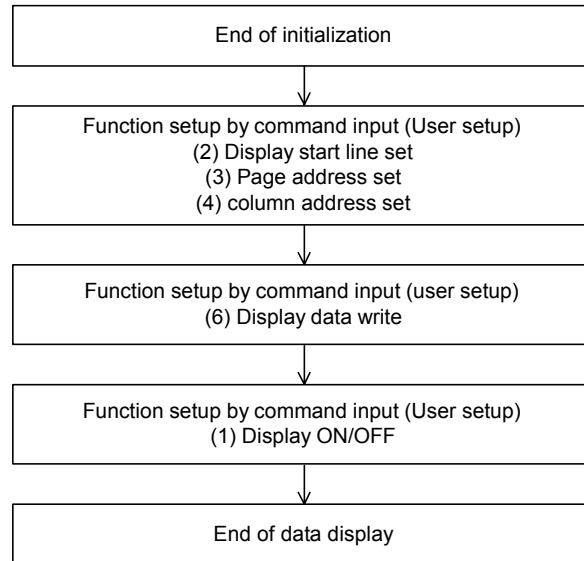
##### 1.1. When the built-in power is being used immediately after turning on the power:



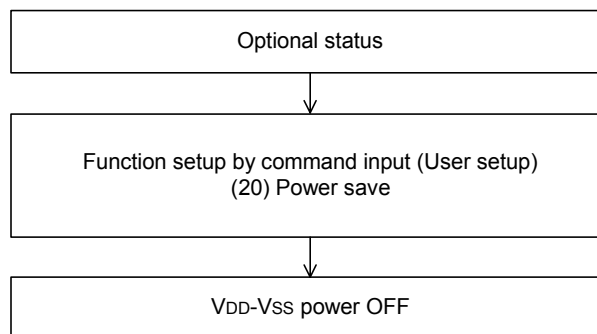
## 1.2. When the built-in power is not being used immediately after turning on the power



## 2. Data Display



## 3. Power OFF



### Absolute Maximum Rating

DC Supply Voltage (VDD, VDD2, VDD3) .....	-0.3V to +4.0V
DC Supply Voltage (VOUT) .....	-0.3V to +15.0V
DC Supply Voltage (V0) .....	-0.3V to +15.0V
Input Voltage (Vin) .....	-0.3V to VDD+0.3V
Operating Ambient Temperature .....	-40°C to +85°C
Storage Temperature .....	-55°C to +125°C

#### \*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### Electrical Characteristics

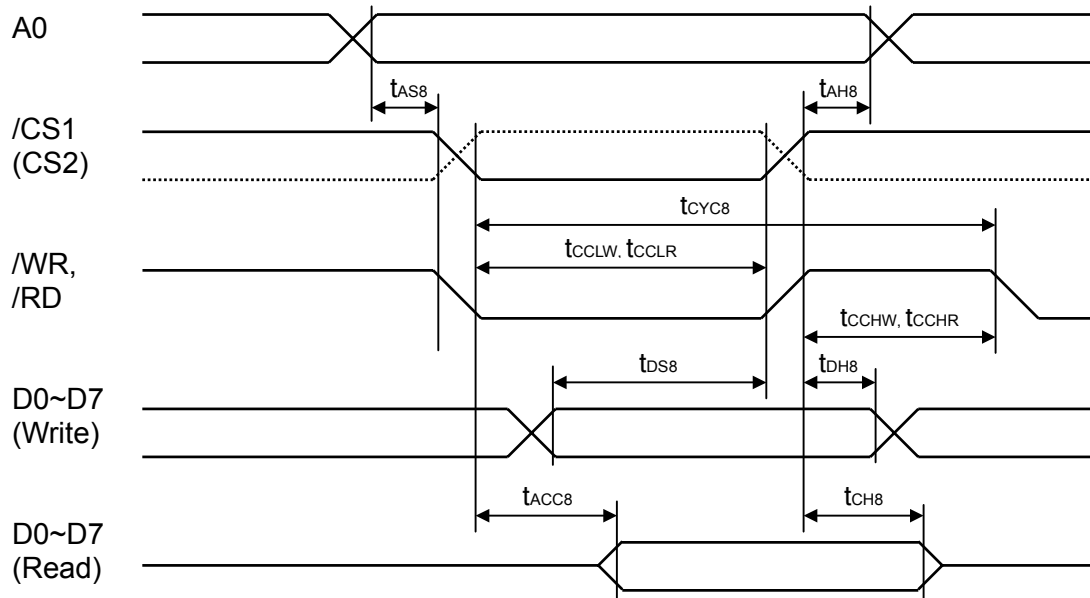
#### DC Characteristics (VSS = 0V, VDD = 1.8 ~ 3.6V, Ta = -40 ~ +85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD VDD3	Operating Voltage	1.8	-	3.6	V	
VDD2	Operating Voltage	1.8	-	3.6	V	2X, 3X boosting
		1.8	-	3.3		4X boosting
		1.8	-	2.8		5X boosting
VOUT	Booster Voltage	6.0	-	14.2	V	
V0	Voltage Regulator Operating Voltage	4.0	-	14.2	V	
VREG	Reference Voltage	2.04	2.10	2.16	V	Ta = 25°C, -0.05%/°C
IDD	Current Consumption	-	20	35	μA	VDD = 3V, V0 = 11V, built-in boosting power supply off, display on, display data = checker and no access, Ta = 25°C
		-	90	160	μA	VDD, VDD2 = 3V, V0 = 11V, 4X built-in boosting power supply, display on, display data = checker and no access, temperature gradient is -0.05%/°C, Ta = 25°C, V0 voltage internal resistor is used, /HPM = 1 (normal power mode).
		-	150	255	μA	VDD, VDD2 = 3V, V0 = 11V, 4X built-in boosting power supply, display on, display data = checker and no access, temperature gradient is -0.05%/°C, Ta = 25°C, V0 voltage internal resistor is used, /HPM = 0 (high power mode).

**DC Characteristics (continued)**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
ISP	Sleep Mode Current Consumption	-	0.01	5	μA	During sleep, Ta = 25°C	
ISB	Standby Mode Current Consumption	-	4	8	μA	During standby, Ta = 25°C	
VIHC	High-Level Input Voltage	0.8 x VDD	-	VDD	V	A0, D0 - D7, /RD (E), /WR (R/W), /CS1, CS2, CLS, CL, FR, M/S, C86, P/S, /DOF, /RES, IRS and /HPM	
VILC	Low-Level Input Voltage	VSS	-	0.2 x VDD	V		
VOHC	High-Level Output Voltage	0.8 x VDD	-	VDD	V	IOH = -0.5mA (D0 - D7, FR, FRS, /DOF, and CL)	
VOLC	Low -Level Output Voltage	VDD	-	0.2 x VDD	V	IOL = 0.5mA (D0 - D7, FR, FRS, /DOF, and CL)	
ILI	Input Leakage Current	-1.0	-	1.0	μA	Vin = VDD or VSS (A0, /RD (E), /WR (R/W), /CS1, CS2, CLS, M/S, C86, P/S, IRS and /RES)	
IHZ	HZ Leakage Current	-3.0	-	3.0	μA	When the D0 - D7, FR, CL, and /DOF are in high impedance	
RON1	LCD Driver ON Resistance	-	2.0	3.5	KΩ	V0 = 11.0V	Ta = 25°C, These are the resistance values for when a 0.1V voltage is applied between the output terminals SEGn or COMn and the various power supply terminal (V0, V1, V2, V3, V4)
RON2	LCD Driver ON Resistance	-	3.2	5.4	KΩ	V0 = 8.0V	
CIN	Input Pad Capacity	-	5.0	8.0	pF	Ta = 25°C, f = 1MHz	
fFRM	Frame Frequency	78.0	80.5	83.0	Hz	fOSC = 31.4 KHz, 1/65duty VDD = 1.8~3.6V	
		64.9	67.4	69.9	Hz	fOSC = 26.3 KHz, 1/65duty VDD = 1.8~3.6V	

Notes: 1. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS2 must always be satisfied.

**AC Characteristics**
**1. System Buses Read/Write Characteristics (for 8080 Series MPU)**


(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

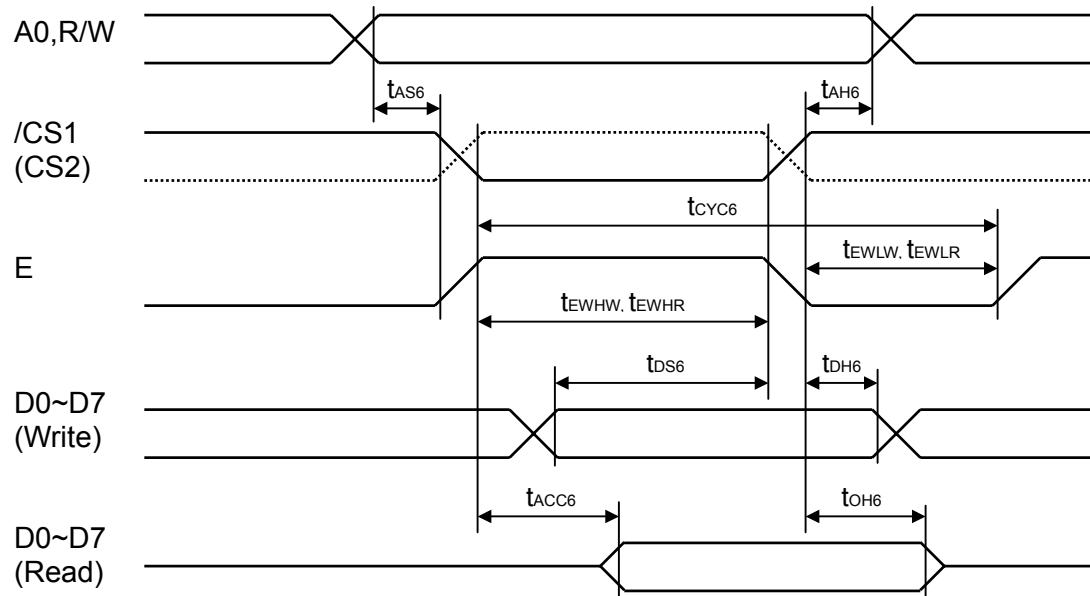
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T <sub>AH8</sub>	Address hold time	0	-	-	ns	A0
T <sub>AS8</sub>	Address setup time	0	-	-	ns	
t <sub>CYC8</sub>	System cycle time	240	-	-	ns	
t <sub>CCLW</sub>	Control low pulse width (write)	90	-	-	ns	/WR
t <sub>CCLR</sub>	Control low pulse width (read)	120	-	-	ns	/RD
t <sub>CCHW</sub>	Control high pulse width (write)	100	-	-	ns	/WR
t <sub>CCHR</sub>	Control high pulse width (read)	60	-	-	ns	/RD
T <sub>DS8</sub>	Data setup time	40	-	-	ns	D0~D7
T <sub>DH8</sub>	Data hold time	10	-	-	ns	
t <sub>ACC8</sub>	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T <sub>CH8</sub>	Output disable time	5	-	50	ns	

## System Buses Read/Write Characteristics (for 8080 Series MPU) (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t <sub>AH8</sub>	Address hold time	0	-	-	ns	A0
t <sub>AS8</sub>	Address setup time	0	-	-	ns	
t <sub>CYC8</sub>	System cycle time	400	-	-	ns	
t <sub>CCLW</sub>	Control low pulse width (write)	150	-	-	ns	/WR
t <sub>CCLR</sub>	Control low pulse width (read)	150	-	-	ns	/RD
t <sub>CCHW</sub>	Control high pulse width (write)	120	-	-	ns	/WR
t <sub>CCHR</sub>	Control high pulse width (read)	120	-	-	ns	/RD
t <sub>DS8</sub>	Data setup time	80	-	-	ns	D0~D7
t <sub>DH8</sub>	Data hold time	30	-	-	ns	
t <sub>ACC8</sub>	/RD access time	-	-	240	ns	D0~D7, CL = 100pF
t <sub>CH8</sub>	Output disable time	10	-	100	ns	

- \*1. The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15ns or less.  
 $(t_r + t_f) < (t_{CYC8} - t_{CCLW} - t_{CCHW})$  for write,  $(t_r + t_f) < (t_{CYC8} - t_{CCLR} - t_{CCHR})$  for read.
- \*2. All timing is specified using 20% and 80% of VDD as the reference.
- \*3. t<sub>CCLW</sub> and t<sub>CCLR</sub> are specified as the overlap interval when /CS1 is low (CS2 is high) and /WR or /RD is low.

**2. System Buses Read/Write Characteristics (for 6800 Series MPU)**


(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t <sub>AH6</sub>	Address hold time	0	-	-	ns	A0, R/W
t <sub>AS6</sub>	Address setup time	0	-	-	ns	
t <sub>CYC6</sub>	System cycle time	240	-	-	ns	
t <sub>EWHW</sub>	Control high pulse width (write)	90	-	-	ns	E
t <sub>EWHR</sub>	Control high pulse width (read)	120	-	-	ns	E
t <sub>EWLW</sub>	Control low pulse width (write)	100	-	-	ns	E
t <sub>EWLR</sub>	Control low pulse width (read)	60	-	-	ns	E
t <sub>DS6</sub>	Data setup time	40	-	-	ns	D0~D7
t <sub>DH6</sub>	Data hold time	10	-	-	ns	
t <sub>ACC6</sub>	/RD access time	-	-	140	ns	D0~D7 CL = 100pF
t <sub>OH6</sub>	Output disable time	5	-	50	ns	

## System Buses Read/Write Characteristics (for 6800 Series MPU) (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t <sub>AH6</sub>	Address hold time	0	-	-	ns	A0, R/W
t <sub>AS6</sub>	Address setup time	0	-	-	ns	
t <sub>CYC6</sub>	System cycle time	400	-	-	ns	
t <sub>EWHW</sub>	Control high pulse width (write)	150	-	-	ns	E
t <sub>EWHR</sub>	Control high pulse width (read)	150	-	-	ns	E
t <sub>EWLW</sub>	Control low pulse width (write)	120	-	-	ns	E
t <sub>EWLR</sub>	Control low pulse width (read)	120	-	-	ns	E
t <sub>DS6</sub>	Data setup time	80	-	-	ns	D0~D7
t <sub>DH6</sub>	Data hold time	30	-	-	ns	
t <sub>ACC6</sub>	/RD access time	-	-	240	ns	D0~D7 CL = 100pF
t <sub>OH6</sub>	Output disable time	10	-	100	ns	

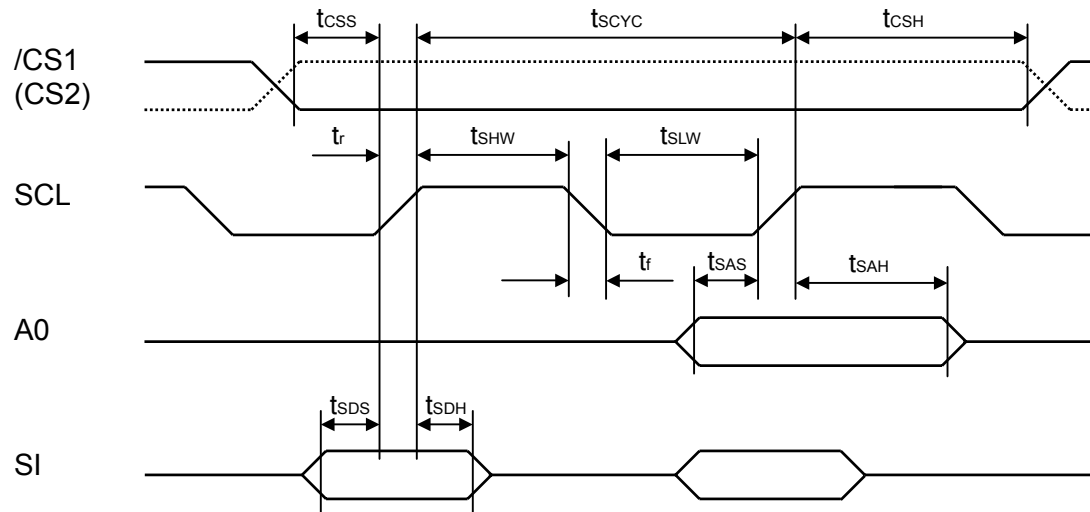
\*1. The input signal rise time and fall time (t<sub>r</sub>, t<sub>f</sub>) is specified at 15ns or less.

(t<sub>r</sub> + t<sub>f</sub>) < (t<sub>CYC6</sub> - t<sub>EWLW</sub> - t<sub>EWHW</sub>) for write, (t<sub>r</sub> + t<sub>f</sub>) < (t<sub>CYC6</sub> - t<sub>EWLR</sub> - t<sub>EWHR</sub>) for read.

\*2. All timing is specified using 20% and 80% of VDD as the reference.

\*3. t<sub>EWHW</sub> and t<sub>EWHR</sub> are specified as the overlap interval when /CS1 is low (CS2 is high) and E is high.

### 3. Serial Interface Timing



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tscyc	Serial clock cycle	120	-	-	ns	SCL
tshw	Serial clock H pulse width	60	-	-	ns	SCL
tslw	Serial clock L pulse width	60	-	-	ns	SCL
tsAS	Address setup time	30	-	-	ns	A0
tsAH	Address hold time	20	-	-	ns	A0
tsDS	Data setup time	30	-	-	ns	SI
tsDH	Data hold time	20	-	-	ns	SI
tcss	Chip select setup time	20	-	-	ns	/CS1, CS2
tcsH	Chip select hold time	40	-	-	ns	/CS1, CS2

## Serial Interface Timing (continued)

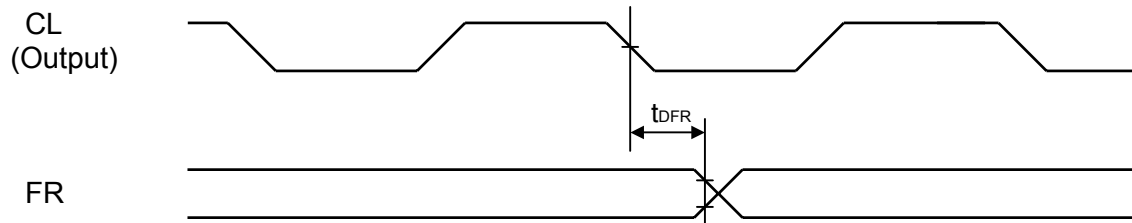
(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tscyc	Serial clock cycle	200	-	-	ns	SCL
tshw	Serial clock H pulse width	80	-	-	ns	SCL
tslw	Serial clock L pulse width	80	-	-	ns	SCL
tsas	Address setup time	60	-	-	ns	A0
tsah	Address hold time	30	-	-	ns	A0
tsds	Data setup time	60	-	-	ns	SI
tsdh	Data hold time	60	-	-	ns	SI
tcss	Chip select setup time	40	-	-	ns	/CS1, CS2
tcsH	Chip select hold time	100	-	-	ns	/CS1, CS2

\*1. The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified as 15ns or less.

\*2. All timing is specified using 20% and 80% of VDD as the standard.

#### 4. Display Control Timing



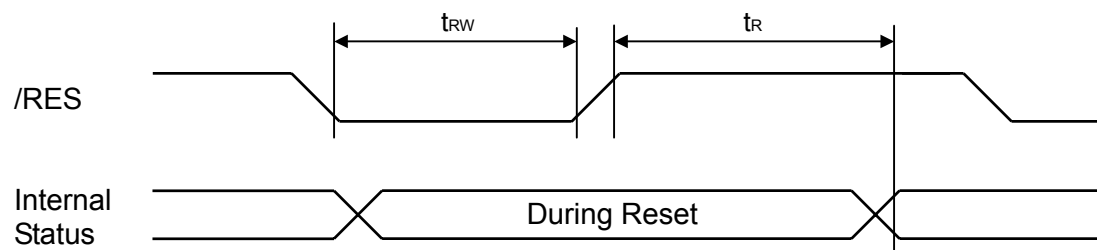
(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$t_{DFR}$	FR delay time	-	20	80	ns	CL = 50 pF

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$t_{DFR}$	FR delay time	-	40	160	ns	CL = 50 pF

#### 5. Reset Timing

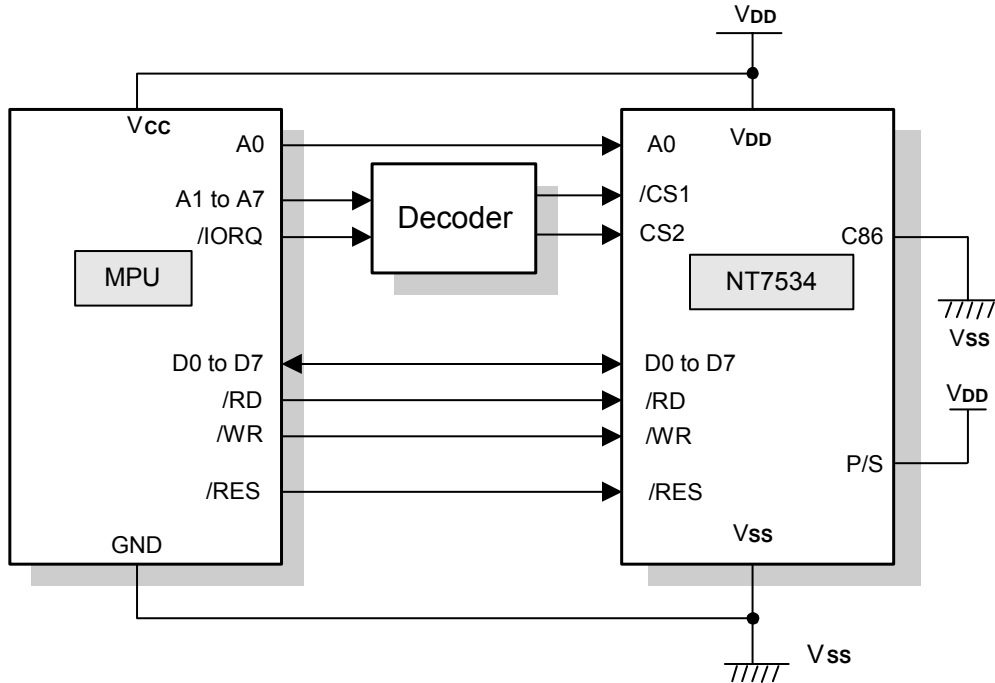
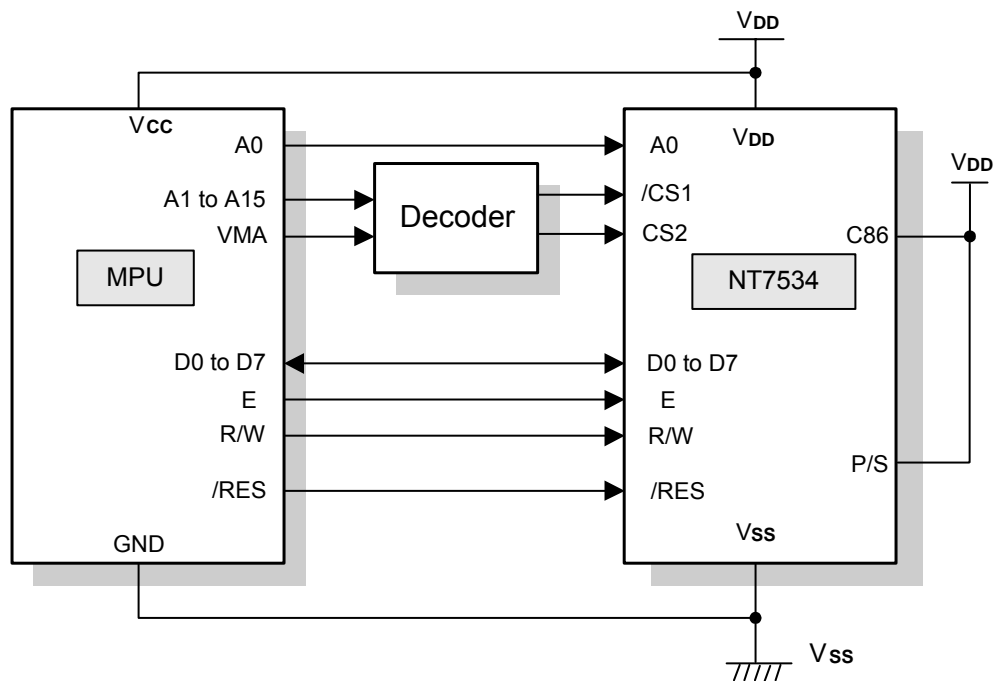


(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$t_R$	Reset Time	-	-	1.0	$\mu$ s	
$t_{RW}$	Reset low pulse width	10	-	-	$\mu$ s	/RES

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

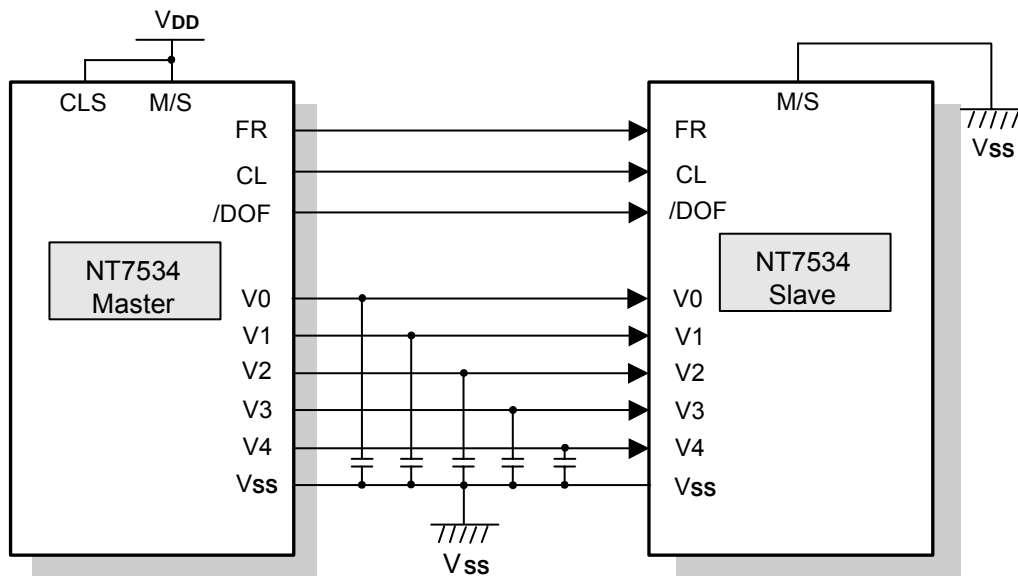
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$t_R$	Reset Time	-	-	2.0	$\mu$ s	
$t_{RW}$	Reset low pulse width	20	-	-	$\mu$ s	/RES

**Microprocessor Interface (for reference only)**
**8080-series microprocessors**

**Figure 9**
**6800-series microprocessors**

**Figure 10**

**Connections between LCD Drivers (for reference only)**

The liquid crystal display area can be enlarged with ease through the use of multiple NT7534 chips. Use same equipment type.

NT7534 (master) ↔ NT7534 (slave)



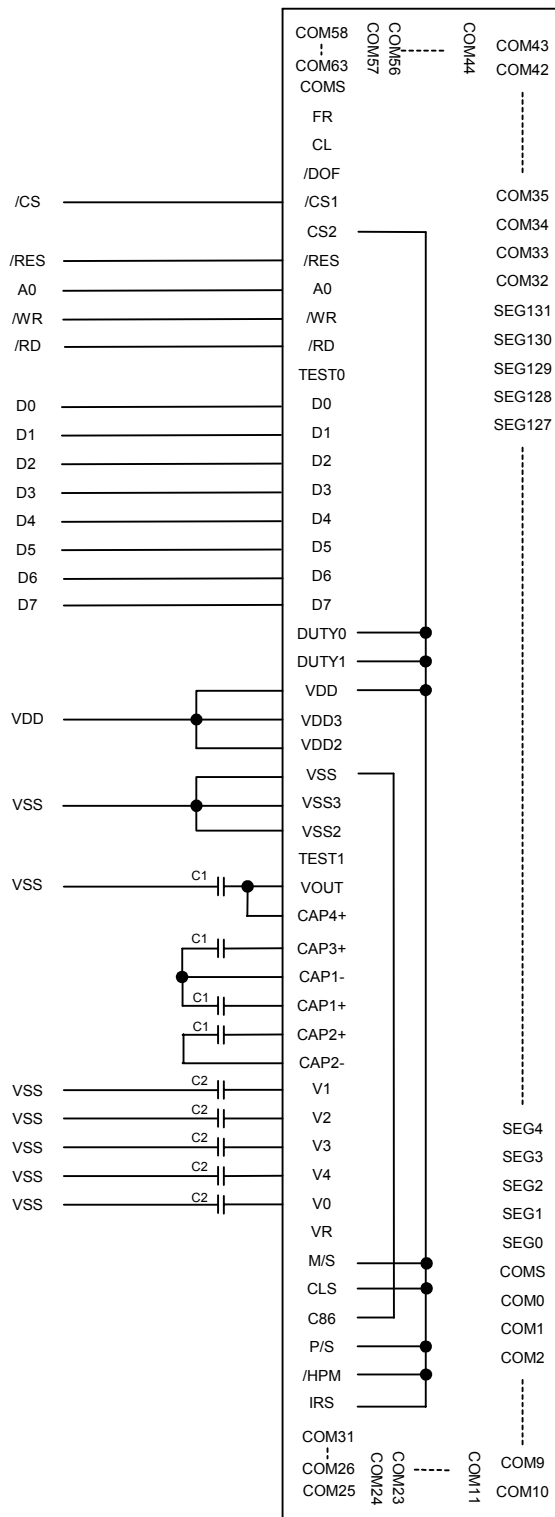
**Figure 11**



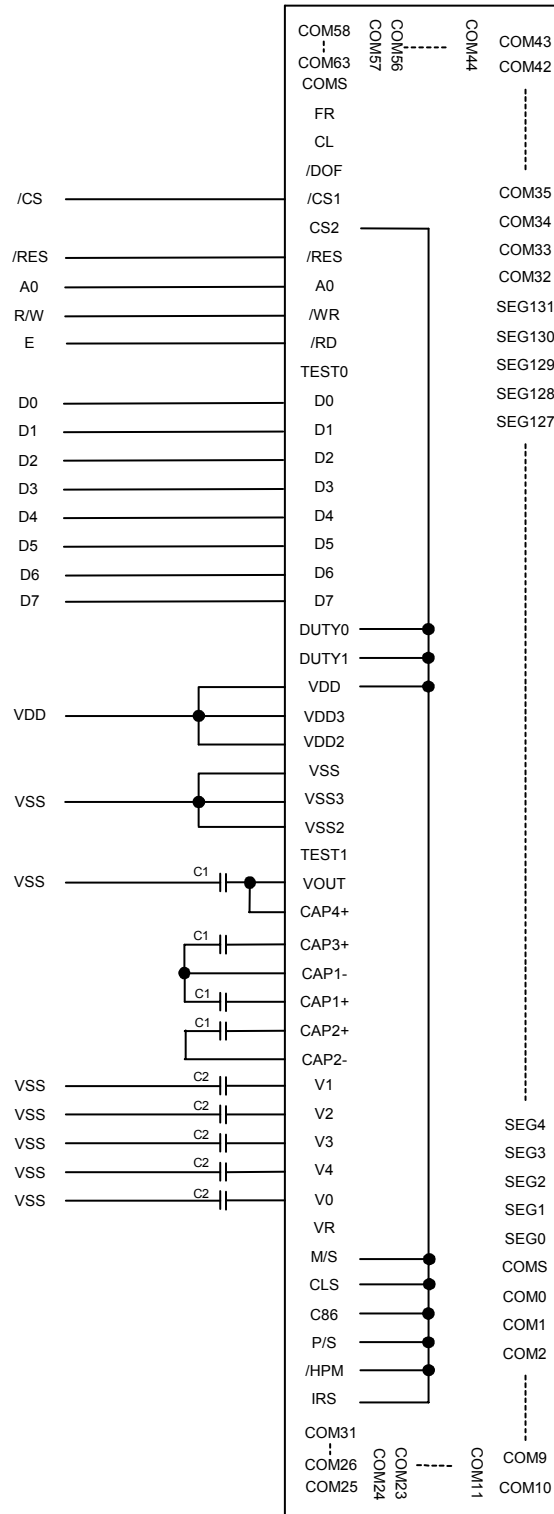


**Application information for Pin Connection to MPU (for reference only)**

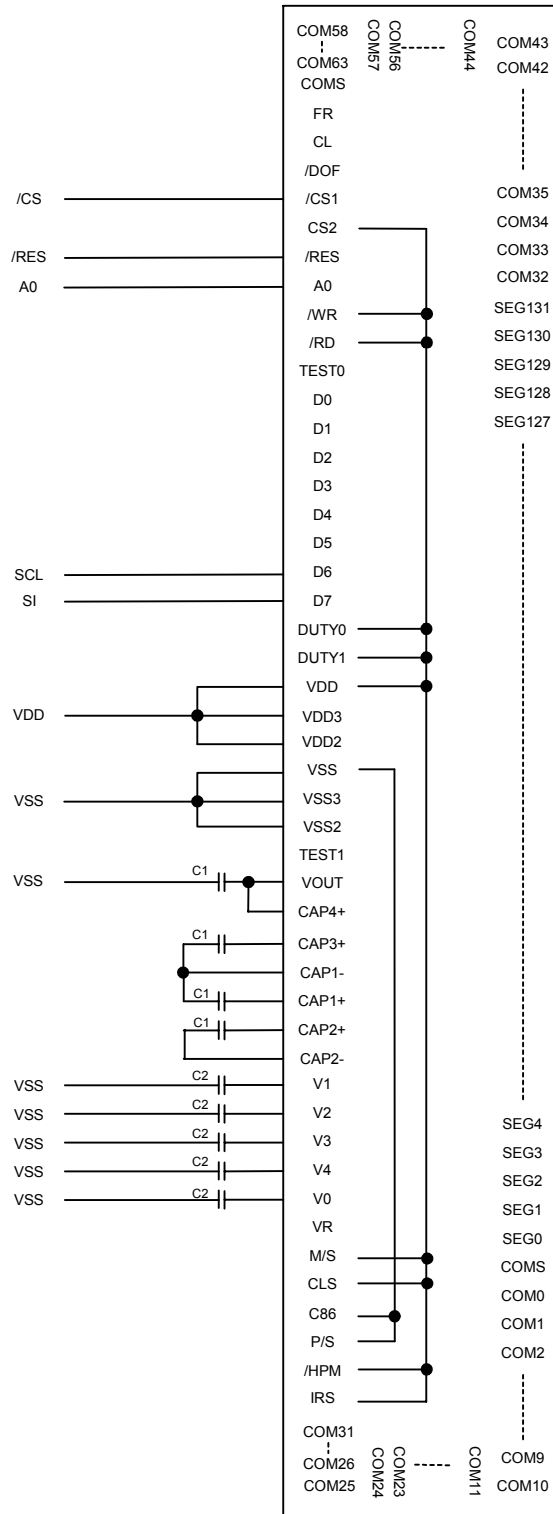
- 8080 MPU Mode: (DUTY0,1 = 11: 1/65duty, M/S = 1: Master mode, CLS = 1: Internal display OSC, /HPM = 1: Normal power mode, IRS = 1: Internal Rb/Ra)

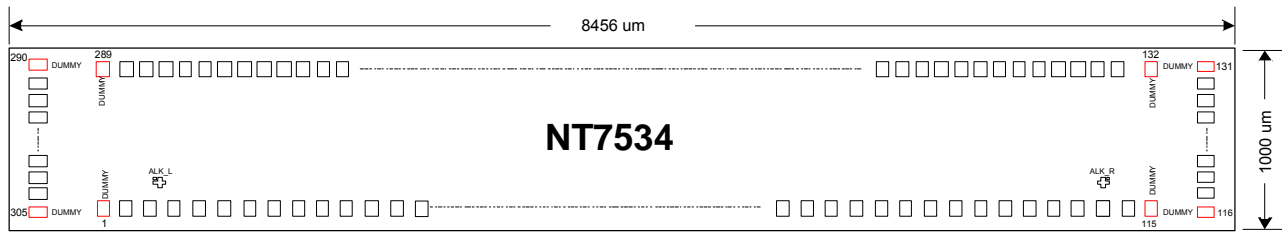


2. 6800 MPU Mode: (DUTY0,1 = 11: 1/65duty, M/S = 1: Master mode, CLS = 1: Internal display OSC, /HPM = 1: Normal power mode, IRS = 1: Internal Rb/Ra)



3. Serial Mode: (DUTY0,1 = 11: 1/65duty, M/S = 1: Master mode, CLS = 1: Internal display OSC, /HPM = 1: Normal power mode, IRS = 1: Internal Rb/Ra)



**Bonding Diagram**


Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY	-3938	-360	30	D3	-1925	-360
2	COM58	-3883	-360	31	D4	-1855	-360
3	COM59	-3833	-360	32	D4	-1785	-360
4	COM60	-3783	-360	33	D5	-1715	-360
5	COM61	-3733	-360	34	D5	-1645	-360
6	COM62	-3683	-360	35	D6	-1575	-360
7	COM63	-3633	-360	36	D6	-1505	-360
8	COMS	-3583	-360	37	D7	-1435	-360
9	FRS	-3465	-360	38	D7	-1365	-360
10	FR	-3395	-360	39	DUTY0	-1295	-360
11	CL	-3325	-360	40	VSS	-1225	-360
12	/DOF	-3255	-360	41	DUTY1	-1155	-360
13	VSS	-3185	-360	42	VDD	-1085	-360
14	/CS1	-3115	-360	43	VDD	-1015	-360
15	CS2	-3045	-360	44	VDD	-945	-360
16	VDD	-2975	-360	45	VDD3	-875	-360
17	/RES	-2835	-360	46	VDD2	-805	-360
18	A0	-2765	-360	47	VDD2	-735	-360
19	/WR	-2695	-360	48	VDD2	-665	-360
20	TEST0	-2625	-360	49	VDD2	-595	-360
21	/RD	-2555	-360	50	VSS	-525	-360
22	VDD	-2485	-360	51	VSS	-455	-360
23	D0	-2415	-360	52	VSS	-385	-360
24	D0	-2345	-360	53	VSS3	-315	-360
25	D1	-2275	-360	54	VSS2	-245	-360
26	D1	-2205	-360	55	VSS2	-175	-360
27	D2	-2135	-360	56	VSS2	-105	-360
28	D2	-2065	-360	57	VSS2	-35	-360
29	D3	-1995	-360	58	TEST1	35	-360

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
59	VOUT	105	-360	95	V0	2625	-360
60	VOUT	175	-360	96	VR	2695	-360
61	VOUT	245	-360	97	VDD	2765	-360
62	CAP4+	315	-360	98	M/S	2835	-360
63	CAP4+	385	-360	99	CLS	2905	-360
64	CAP4+	455	-360	100	VSS	2975	-360
65	CAP4+	525	-360	101	C86	3045	-360
66	CAP3+	595	-360	102	P/S	3115	-360
67	CAP3+	665	-360	103	VDD	3185	-360
68	CAP3+	735	-360	104	/HPM	3255	-360
69	CAP3+	805	-360	105	VSS	3325	-360
70	CAP1-	875	-360	106	IRS	3395	-360
71	CAP1-	945	-360	107	VDD	3465	-360
72	CAP1-	1015	-360	108	COM31	3583	-360
73	CAP1-	1085	-360	109	COM30	3633	-360
74	CAP1+	1155	-360	110	COM29	3683	-360
75	CAP1+	1225	-360	111	COM28	3733	-360
76	CAP1+	1295	-360	112	COM27	3783	-360
77	CAP1+	1365	-360	113	COM26	3833	-360
78	CAP2+	1435	-360	114	COM25	3883	-360
79	CAP2+	1505	-360	115	DUMMY	3938	-360
80	CAP2+	1575	-360	116	DUMMY	4088	-380
81	CAP2+	1645	-360	117	COM24	4088	-325
82	CAP2-	1715	-360	118	COM23	4088	-275
83	CAP2-	1785	-360	119	COM22	4088	-225
84	CAP2-	1855	-360	120	COM21	4088	-175
85	CAP2-	1925	-360	121	COM20	4088	-125
86	V1	1995	-360	122	COM19	4088	-75
87	V1	2065	-360	123	COM18	4088	-25
88	V2	2135	-360	124	COM17	4088	25
89	V2	2205	-360	125	COM16	4088	75
90	V3	2275	-360	126	COM15	4088	125
91	V3	2345	-360	127	COM14	4088	175
92	V4	2415	-360	128	COM13	4088	225
93	V4	2485	-360	129	COM12	4088	275
94	V0	2555	-360	130	COM11	4088	325

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
131	DUMMY	4088	380	167	SEG22	2175	360
132	DUMMY	3938	360	168	SEG23	2125	360
133	COM10	3883	360	169	SEG24	2075	360
134	COM9	3833	360	170	SEG25	2025	360
135	COM8	3783	360	171	SEG26	1975	360
136	COM7	3733	360	172	SEG27	1925	360
137	COM6	3683	360	173	SEG28	1875	360
138	COM5	3633	360	174	SEG29	1825	360
139	COM4	3583	360	175	SEG30	1775	360
140	COM3	3533	360	176	SEG31	1725	360
141	COM2	3483	360	177	SEG32	1675	360
142	COM1	3433	360	178	SEG33	1625	360
143	COM0	3383	360	179	SEG34	1575	360
144	COMS	3333	360	180	SEG35	1525	360
145	SEG0	3275	360	181	SEG36	1475	360
146	SEG1	3225	360	182	SEG37	1425	360
147	SEG2	3175	360	183	SEG38	1375	360
148	SEG3	3125	360	184	SEG39	1325	360
149	SEG4	3075	360	185	SEG40	1275	360
150	SEG5	3025	360	186	SEG41	1225	360
151	SEG6	2975	360	187	SEG42	1175	360
152	SEG7	2925	360	188	SEG43	1125	360
153	SEG8	2875	360	189	SEG44	1075	360
154	SEG9	2825	360	190	SEG45	1025	360
155	SEG10	2775	360	191	SEG46	975	360
156	SEG11	2725	360	192	SEG47	925	360
157	SEG12	2675	360	193	SEG48	875	360
158	SEG13	2625	360	194	SEG49	825	360
159	SEG14	2575	360	195	SEG50	775	360
160	SEG15	2525	360	196	SEG51	725	360
161	SEG16	2475	360	197	SEG52	675	360
162	SEG17	2425	360	198	SEG53	625	360
163	SEG18	2375	360	199	SEG54	575	360
164	SEG19	2325	360	200	SEG55	525	360
165	SEG20	2275	360	201	SEG56	475	360
166	SEG21	2225	360	202	SEG57	425	360

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
203	SEG58	375	360	239	SEG94	-1425	360
204	SEG59	325	360	240	SEG95	-1475	360
205	SEG60	275	360	241	SEG96	-1525	360
206	SEG61	225	360	242	SEG97	-1575	360
207	SEG62	175	360	243	SEG98	-1625	360
208	SEG63	125	360	244	SEG99	-1675	360
209	SEG64	75	360	245	SEG100	-1725	360
210	SEG65	25	360	246	SEG101	-1775	360
211	SEG66	-25	360	247	SEG102	-1825	360
212	SEG67	-75	360	248	SEG103	-1875	360
213	SEG68	-125	360	249	SEG104	-1925	360
214	SEG69	-175	360	250	SEG105	-1975	360
215	SEG70	-225	360	251	SEG106	-2025	360
216	SEG71	-275	360	252	SEG107	-2075	360
217	SEG72	-325	360	253	SEG108	-2125	360
218	SEG73	-375	360	254	SEG109	-2175	360
219	SEG74	-425	360	255	SEG110	-2225	360
220	SEG75	-475	360	256	SEG111	-2275	360
221	SEG76	-525	360	257	SEG112	-2325	360
222	SEG77	-575	360	258	SEG113	-2375	360
223	SEG78	-625	360	259	SEG114	-2425	360
224	SEG79	-675	360	260	SEG115	-2475	360
225	SEG80	-725	360	261	SEG116	-2525	360
226	SEG81	-775	360	262	SEG117	-2575	360
227	SEG82	-825	360	263	SEG118	-2625	360
228	SEG83	-875	360	264	SEG119	-2675	360
229	SEG84	-925	360	265	SEG120	-2725	360
230	SEG85	-975	360	266	SEG121	-2775	360
231	SEG86	-1025	360	267	SEG122	-2825	360
232	SEG87	-1075	360	268	SEG123	-2875	360
233	SEG88	-1125	360	269	SEG124	-2925	360
234	SEG89	-1175	360	270	SEG125	-2975	360
235	SEG90	-1225	360	271	SEG126	-3025	360
236	SEG91	-1275	360	272	SEG127	-3075	360
237	SEG92	-1325	360	273	SEG128	-3125	360
238	SEG93	-1375	360	274	SEG129	-3175	360

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
275	SEG130	-3225	360	292	COM45	-4088	275
276	SEG131	-3275	360	293	COM46	-4088	225
277	COM32	-3333	360	294	COM47	-4088	175
278	COM33	-3383	360	295	COM48	-4088	125
279	COM34	-3433	360	296	COM49	-4088	75
280	COM35	-3483	360	297	COM50	-4088	25
281	COM36	-3533	360	298	COM51	-4088	-25
282	COM37	-3583	360	299	COM52	-4088	-75
283	COM38	-3633	360	300	COM53	-4088	-125
284	COM39	-3683	360	301	COM54	-4088	-175
285	COM40	-3733	360	302	COM55	-4088	-225
286	COM41	-3783	360	303	COM56	-4088	-275
287	COM42	-3833	360	304	COM57	-4088	-325
288	COM43	-3883	360	305	DUMMY	-4088	-380
289	DUMMY	-3938	360				
290	DUMMY	-4088	380				
291	COM44	-4088	325				

**Alignment Mark Location (Total: 2 pins)**

NO	X	Y
L	-3830	-100
R	3830	-100

### Package Information



### Pad Dimensions

Item	Pad No.		Size		Unit
			X	Y	
Chip size	-		8456	1000	μm
Chip thickness	-		525		μm
Pad pitch	9 ~ 16, 17 ~ 107		70		μm
	2 ~ 8, 108 ~ 114, 117 ~ 130, 133 ~ 144, 145 ~ 276, 277 ~ 288, 291 ~ 304		50		
	8 ~ 9, 107 ~ 108		118		
	16 ~ 17		140		
	144 ~ 145, 276 ~ 277		58		
	1 ~ 2, 114 ~ 115, 116 ~ 117, 130 ~ 131, 132 ~ 133, 288 ~ 289, 290 ~ 291, 304 ~ 305		55		
Bump size	Output Pad	2 ~ 8, 108 ~ 114, 133 ~ 288,	32	90	μm
		117 ~ 130, 291 ~ 304	90	32	
	Input Pad	9 ~ 107	45	90	
	Dummy Pad	1, 115, 132, 289	40	90	
116, 131, 290, 305		90	40		
Bump height	All pads		15 ± 3		μm

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## Ordering Information

Part No.	Packages
NT7534H-BDT	Gold Bump on Chip Tray
NT7534H-TABF1	48mm Tape Automated Bonding Package
NT7534H-TAB0011	35mm Tape Automated Bonding Package

## Cautions

1. The contents of this document will be subjected to change without notice.
2. Precautions against light projection:

Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.

Observe the following instructions in using this product:

  - a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
  - b. Test and inspect the product under an environment free of light source penetration.
  - c. Confirm that all surfaces around the IC will not be exposed to light source.